TANDEM

NonStop EXP™

1432 Processor Subsystem

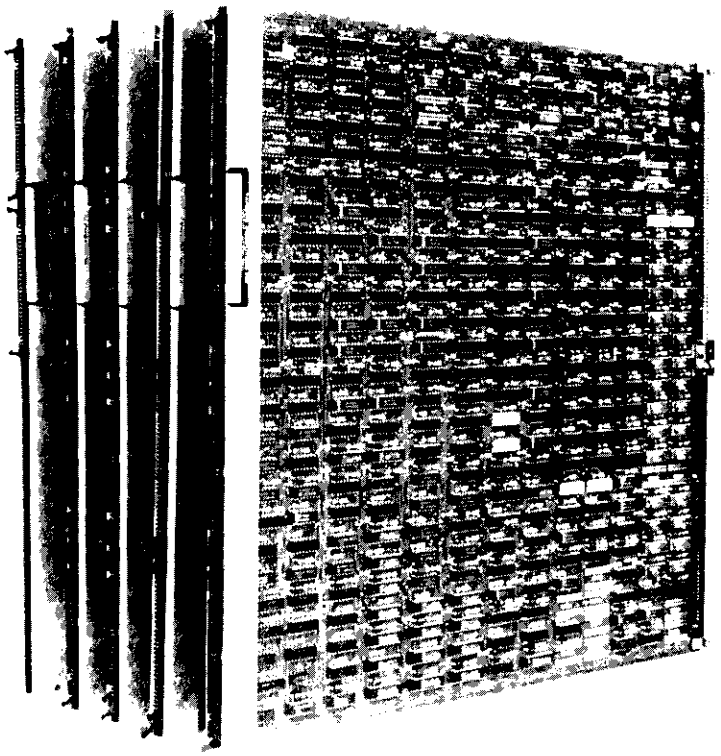
Maintenance Manual

Part No. 82885

MAINTENANCE MANUAL

NonStop TXP (TM)

1432 PROCESSOR SUBSYSTEM



TANDEM COMPUTERS INCORPORATED
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Santa Clara, California 95050

Tandem Part No. 82885

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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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SECTION 1
INTRODUCTION

1.0 INTRODUCTION

The NonStop TXP processor consists of a four-board CPU plus memory. A maximum of four memory boards may be used per CPU. Currently each Memory Board contains 2 MB for a total of 8 MB memory storage capacity. The Processor will address up to 16 MB when denser memory is available.

1.1 REFERENCED DOCUMENTS

Refer to the following documents for additional detailed information not found in this manual.

a. Operations and Service Processor User Guide, Part Number 82801.

b. NonStop II and NonStop TXP Operations and Service Processor Maintenance Manual, Part Number 82846.

c. NonStop II System Description Manual, Part Number 82077.

d. Stress Manual (NonStop and NonStop II), Part Number 82852.

e. CPU1432, NonStop TXP Diagnostic Operating Procedures, Part Number 82804, Volume 1, Chapter 1.

f. MEM2432, NonStop TXP Diagnostic Operating Procedures, Part Number 82804, Volume 1, Chapter 2.

g. System Management Manual, NonStop II, Part Number 82069.

h. NonStop II System Operations Manual, Part Number 82075.

i. NonStop II and NonStop TXP Power Subsystem Manual, Part Number 82807.

j. INSTALLATION GUIDE NonStop II AND NonStop TXP, Part Number 82855.

SECTION 2
PHYSICAL DESCRIPTION

2.0 PHYSICAL DESCRIPTION

The Tandem NonStop TXP processor consists of five new board types: the Instruction Processor (IP), Memory Control (MC), Channel and Control (CC), Sequencer and Control Store (SQ), and the Memory Array (MM) Boards. None of these boards is interchangeable with boards of the NonStop II CPU.

These boards have been logically partitioned to keep critical buses from crossing board boundaries. To improve performance and ease backplane pin limitations the JBUS, KBUS, MBUS, Cache Data Bus, and Address Bus are contained on the IP board.

Figure 2-1 shows the location and board sequence of a NonStop TXP CPU installed in a NonStop II shared system.

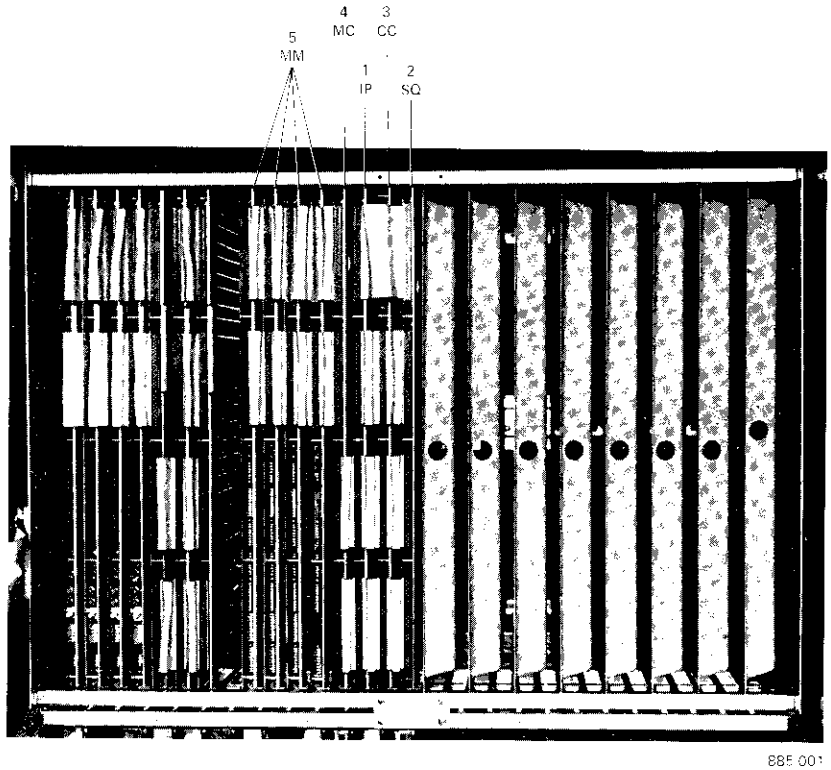


Figure 2-1 NonStop TXP Board Locations

2.1 POWER REQUIREMENTS

Power requirements for a NonStop TXP CPU are +5V IPS (Vcc) at 80 Amps, and +5V UPS (Vuu) at 17.3 Amps. These requirements are met by a single power supply that is not shared with any I/O Controllers. All other power supply information may be found in the NonStop II and NonStop TXP Power Subsystem Manual.

Board power requirements:

a. Instruction Processor Board (IP): +5 Vcc (IPS) = 18 amps

b. Sequencer and Control Store Board (SQ): +5 Vcc (IPS) = 15 amps

c. Channel and Control Board (CC): +5 Vcc (IPS) = 15 amps

d. Memory Control Board (MC): +5 Vcc (IPS) = 14.5 amps
+5 Vuu (UPS) = 1.0 amps

e. Memory Array Board (MM): +5 Vcc (IPS) = 5.1 amps
standby +5 Vuu (UPS) = 3.2 amps
active +5 Vuu (UPS) = 6.7 amps

2.2 OPERATING ENVIRONMENT

The NonStop TXP system operating environment is:

Temperature: 60 to 85 degrees F (15-29 degrees C).

Relative Humidity: 42 to 70 percent (noncondensing).

2.3 CHANNEL AND CONTROL BOARD INDICATORS

The location of the indicators on the Channel and Control (CC) board is illustrated in Figure 2-2. Their purpose is to indicate error codes useful for troubleshooting the CPU. These codes are described in paragraph 5.1.1 and Table 5.1.

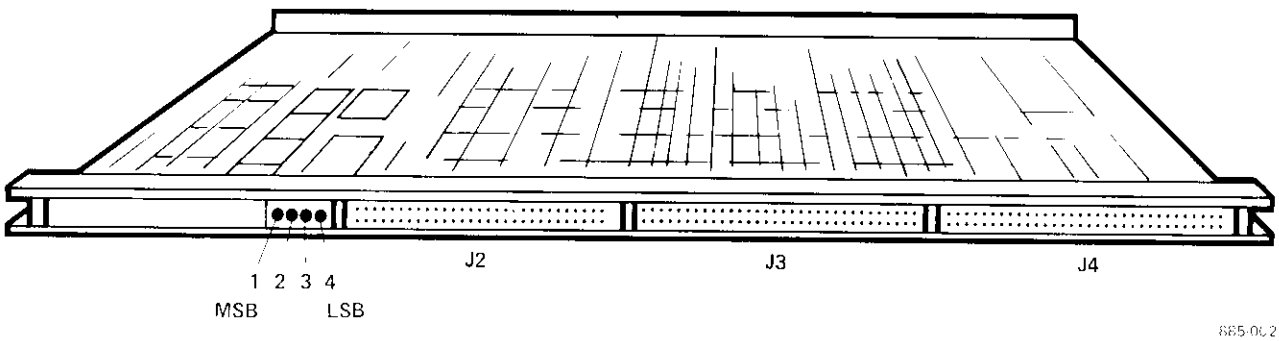


Figure 2-2 CC Board Indicators (front edge)

2.4 PROCESSOR BOARDS

The following paragraphs identify the boards used in the CPU, the functional units on each board, and the expected current drain.

Figure 2-3 shows the NonStop TXP processor board interconnections.

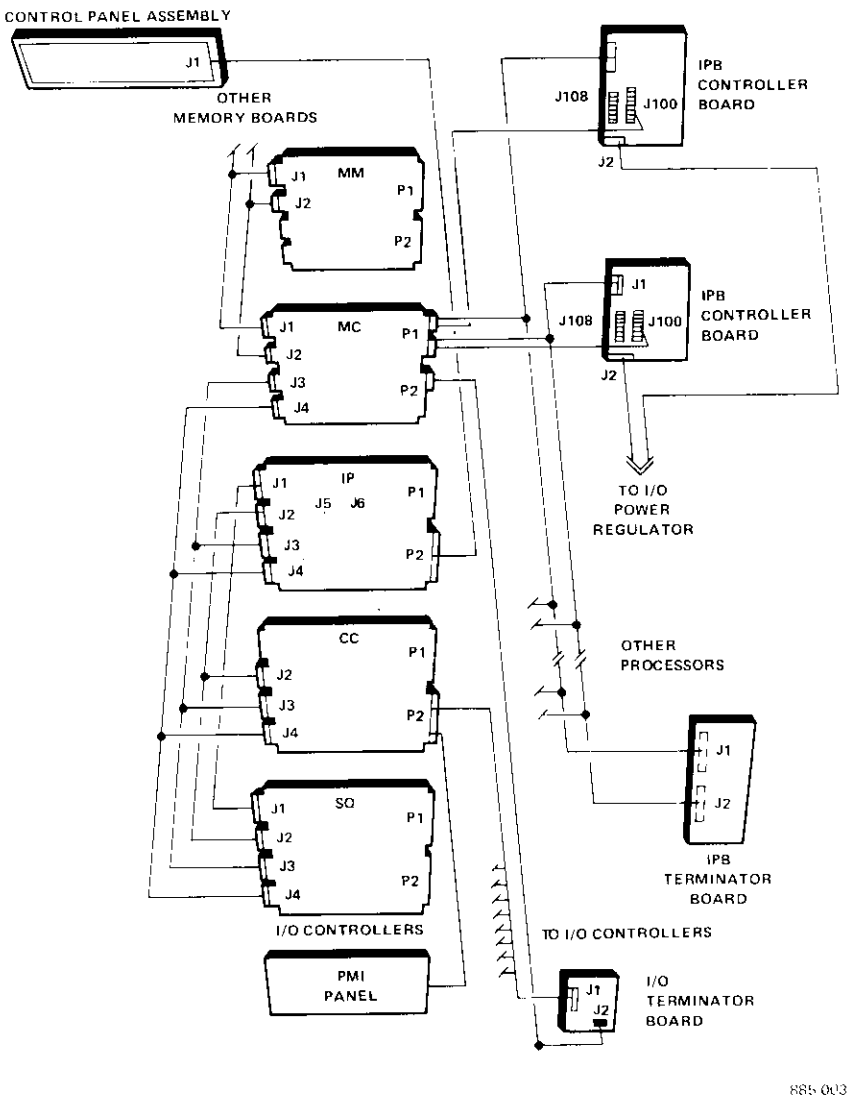


Figure 2-3 NonStop TXP Processor Subsystem Interconnections

2.4.1 Instruction Processing Board (IP)

See Figure 2-1 for the location of the IP board within the CPU card cage. Figure 2-4 shows a board layout of the Instruction Processing Board.

Functional Units:

a. Main Arithmetic Logic Unit (ALU) and Data Path

b. Address Translator

c. Data and Page Table Caches

d. Special Bus Interface

e. Power On (PON) Detection

f. Clock Control

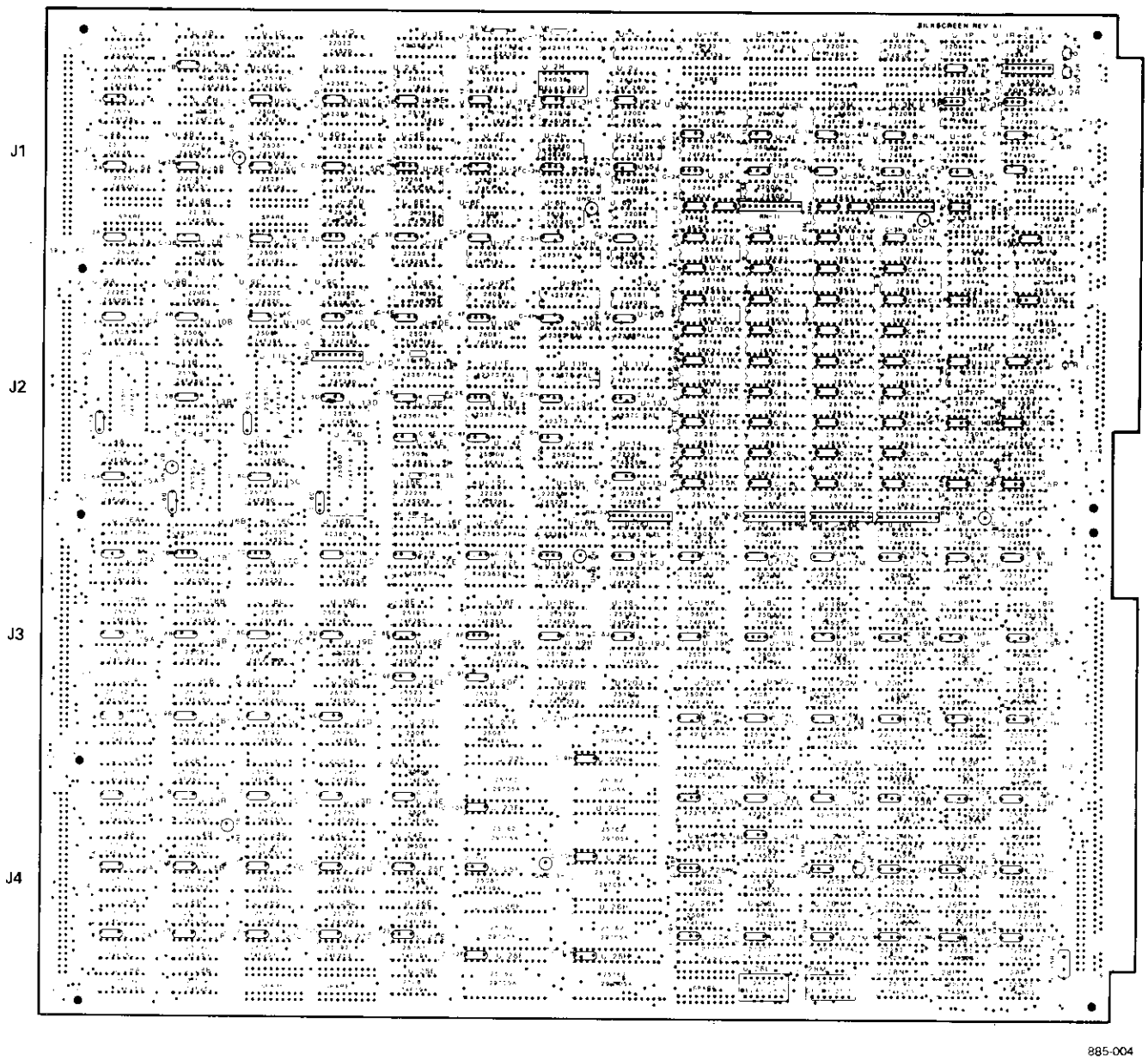


Figure 2-4 Instruction Processor Board

2.4.2 Sequencer and Control Store Board (SQ)

See Figure 2-1 for the location of the SQ board within the CPU card cage. Figure 2-5 shows a board layout of the Sequencer and Control Store board.

Functional Units:

a. Sequencer Control

b. Writable Control Store (WCS)

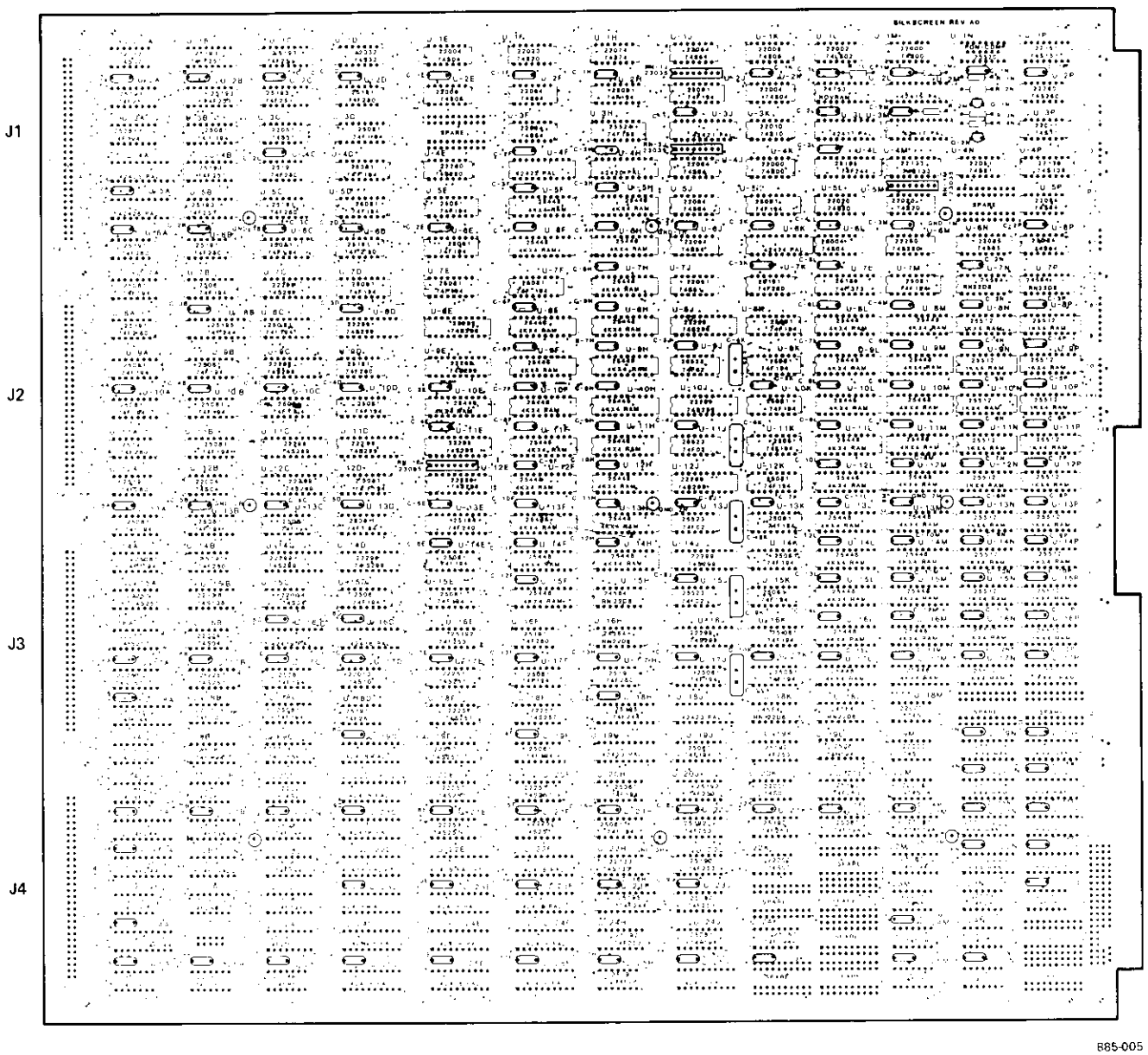


Figure 2-5 Sequencer and Control Store Board

2.4.3 Channel and Control Board (CC)

See Figure 2-1 for the location of the CC board within the CPU card cage. Figure 2-6 shows a board layout of the Channel and Control board.

Functional Units:

a. Channel Logic

b. DDT

c. Interval Timer

d. SALU

e. Mul/Div

f. Scratch Pad Registers

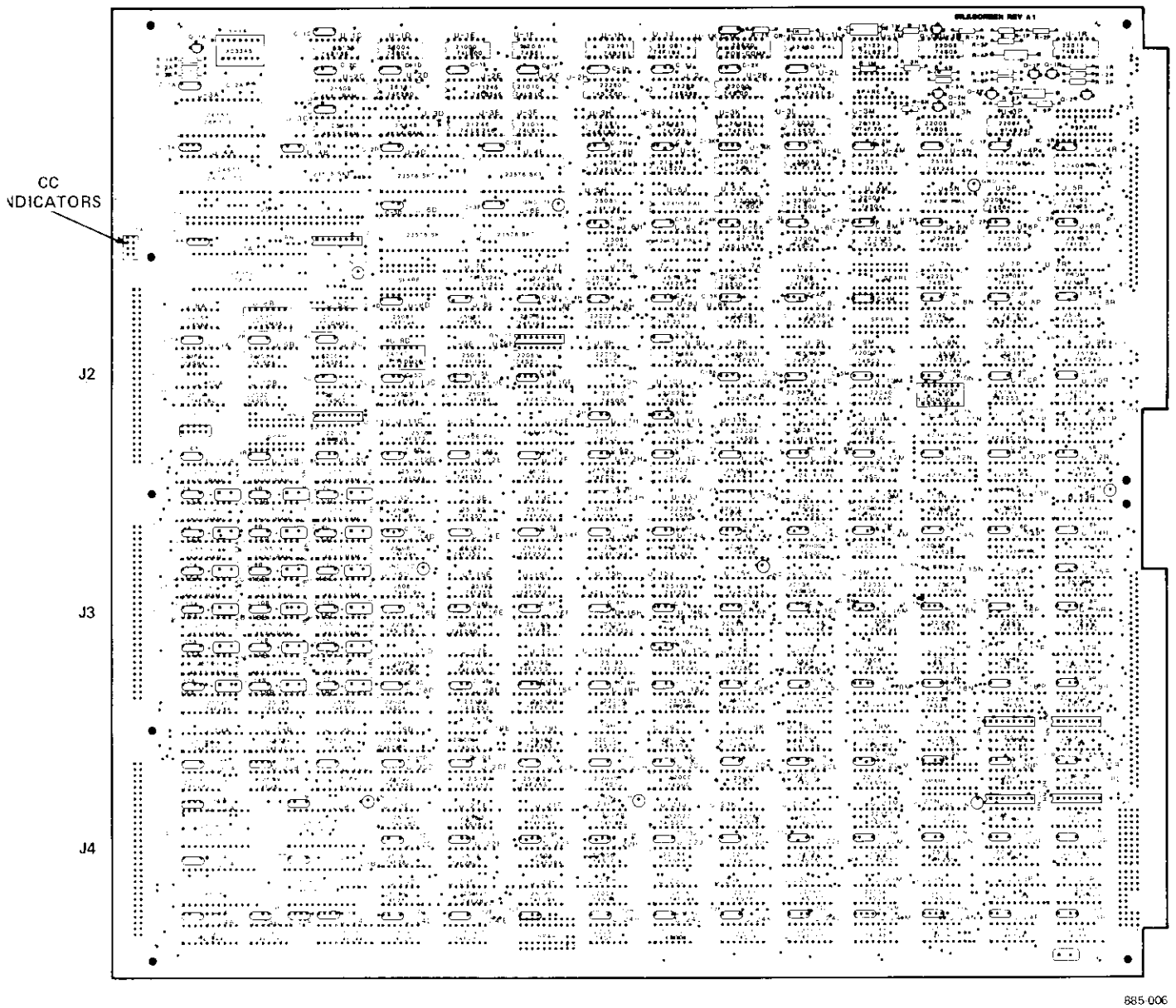


Figure 2-6 Channel and Control Board

2.4.4 Memory Control Board (MC)

See Figure 2-1 for the location of the MC within the CPU card cage. Figure 2-7 shows a board layout of the Memory Control Board.

Functional Units:

a. Memory Control Unit (MCU)

b. IPB circuit

c. System Clock

d. Barrel Shifter

e. Interrupt Logic

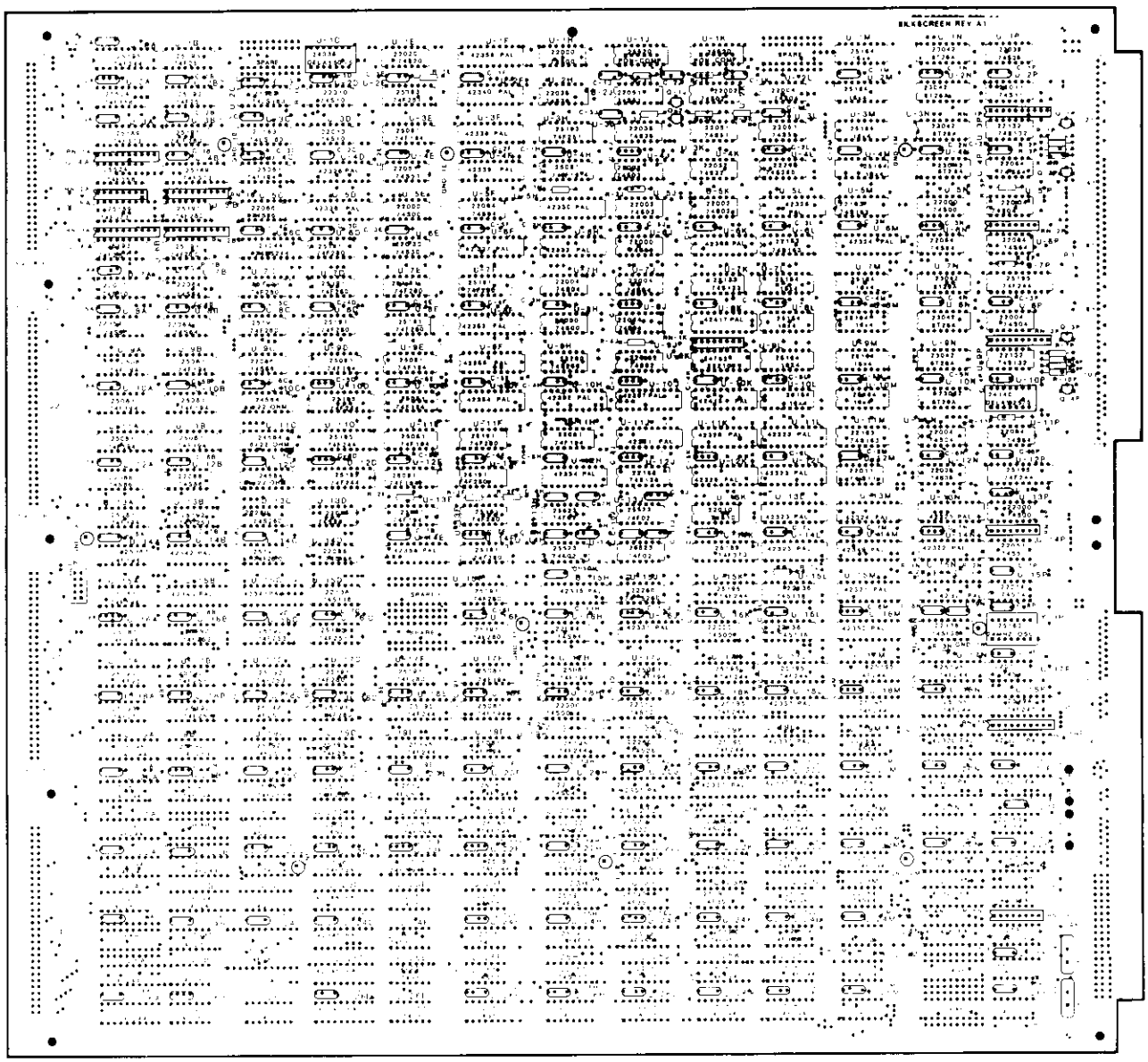


Figure 2-7 Memory Control Board

2.4.5 Memory Array Board (MM)

See Figure 2-1 for the location of the MM board within the CPU card cage. Figure 2-8 shows a board layout of the Memory Array Board.

Functional Units:

a. Main Memory Array

b. Memory Data Register

c. NOVRAMs

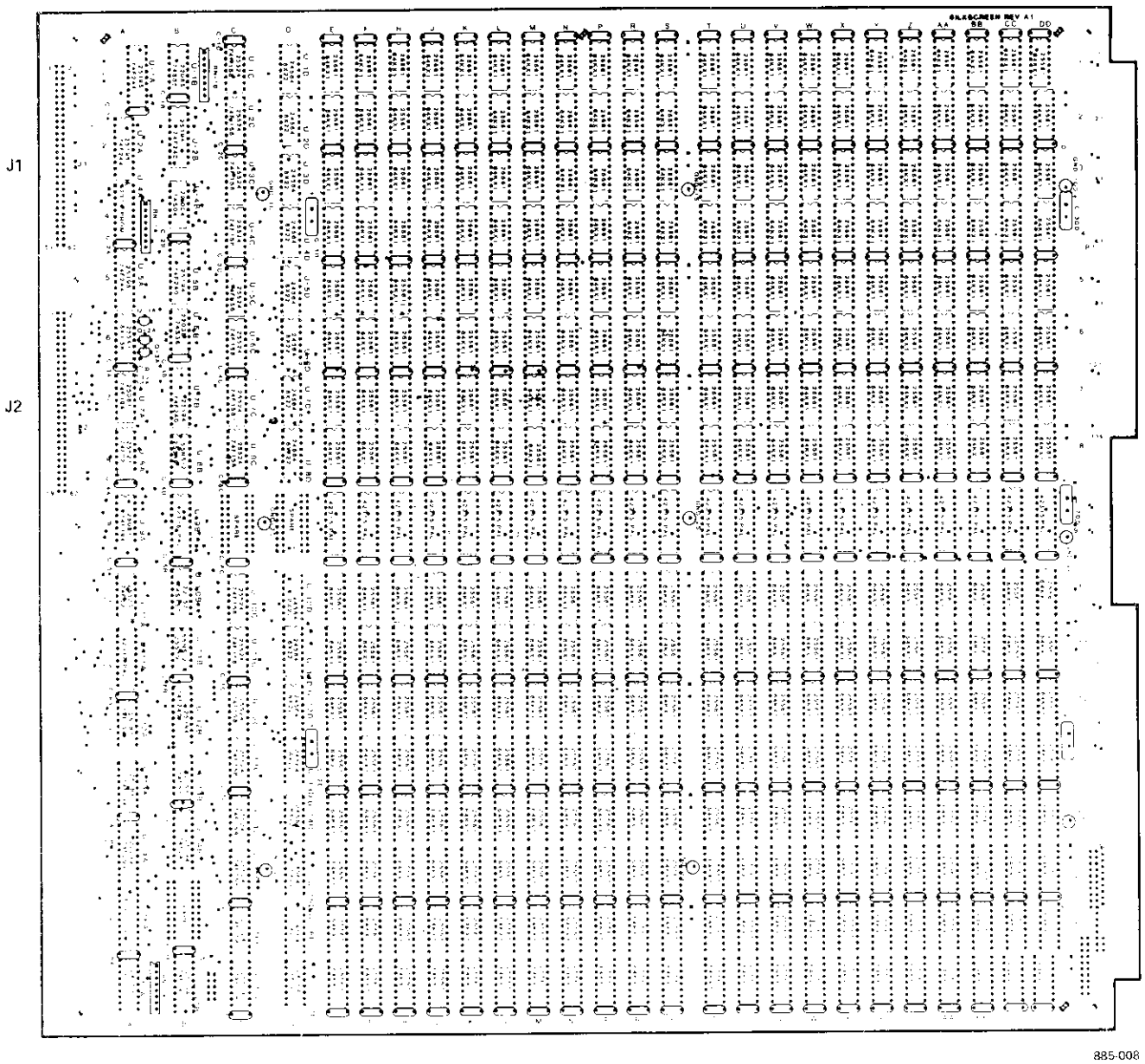


Figure 2-8 Memory Array Board

SECTION 3
FUNCTIONAL DESCRIPTION

3.0 FUNCTIONAL DESCRIPTION

The NonStop TXP system configuration is the same as all previous NonStop (TM) systems. Figure 3-1 shows the diagram of a typical NonStop TXP processor subsystem configuration.

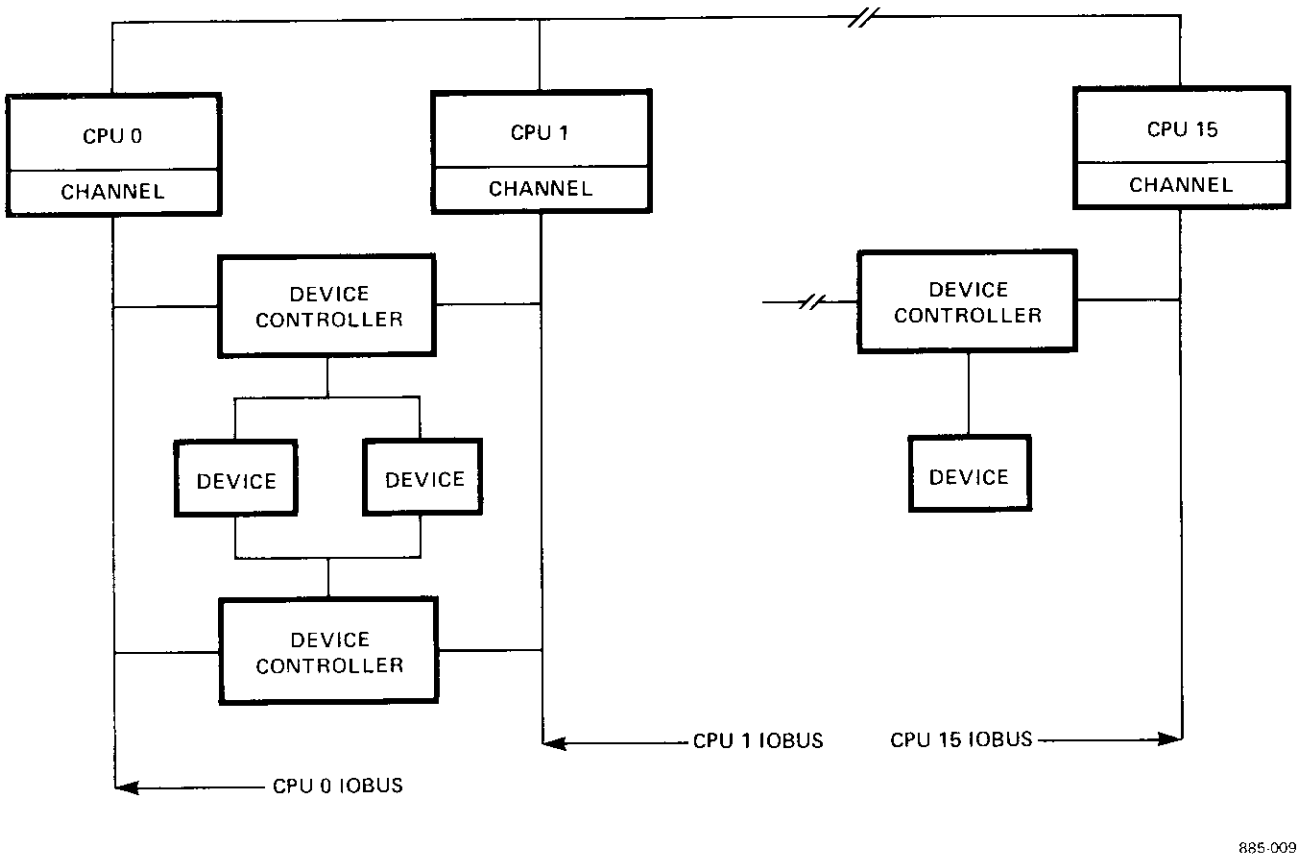


Figure 3-1 Processor Subsystem Configuration

3.1 OPERATIONAL DESCRIPTION

This section provides the user with an operational overview of the processor subsystem. The following paragraphs provide a brief description of each board's functional units.

Figure 3-2 shows a functional block diagram of the NonStop TXP processor subsystem containing the following boards and interconnections:

a. Instruction Processing board (IP)

b. Sequencer and Control Store board (SQ)

c. Channel and Control board (CC)

d. Memory Control board (MC)

e. Memory Array board (MM)

Refer to Figure 3-2 when reviewing the functional units of each board, major circuits, and related processor status screen errors (Processor status errors are indicated in red).

3.1.1 Instruction Processing Board (IP)

The following functional units are located on the IP board:

a. The Main Arithmetic Logic Unit (ALU) supports 16-bit signed and unsigned arithmetic and logical functions, and interfaces to the Special Buses.

   The Data Path has been streamlined to reduce the cycle time of the CPU. There is no shifter in the main data path, and the number of registers driving the J and K buses has been minimized to reduce the loading.

b. The Address Translator shortens the time required to generate extended memory addresses. The translation hardware contributes significantly to the processor's throughput.

c. The memory cache provides parallel, high-speed access to a portion of the data stored in the processor memory array. This arrangement increases throughput by reducing the time the processor waits for data. The memory cache stores up to 64K bytes of non-specific memory data and also the physical address and status of up to 2K memory pages. Both stores are accessed simultaneously under microprogram control. The memory cache performs the following operations when it services a request to access a data word:

   1. Delivers or updates an instruction or operand word

2. Indicates whether any word delivered is correct

3. Issues a physical memory address to the memory controller

4. Reports on the status of the memory page named in the address it issued (including whether or not it contains the requested word).

d. The Special Bus Interface enhances performance by operating in parallel with the main data path.

e. Power-On Detection. This signal is true when the supply voltage to the board is high enough to guarantee proper logic operation (Vcc rises above 4.89 volts and goes false when Vcc drops below 4.775 volts). The IP board sends the PON signal to the CC board, which uses it to generate the RESET signal.

Additional functions of the IP board are:

a. Providing multiple sources for Special Data Paths (SJ and SK buses).

b. Providing multiple sources for the main ALU

c. Receiving data from the special data path (SM bus) for use by the Address Translator, Memory Cache, and main ALU.

d. Accumulating the main ALU results for use by the main ALU, special data paths, Cache and Address Translator.

e. Maintaining conditions codes and the Environment Register

f. Maintaining the Register Stack, certain dedicated registers (L, S, XBLS, XLLS), and four scratch registers (SA, SB, SC, SD)

Figure 3-2 shows the IP board interconnections, functional units, major circuits, and related processor status screen errors.

3.1.2 Sequencer and Control Store Board (SQ)

The following functional units are located on the SQ board:

a. The Sequencer (microcode sequencing logic) fetches microinstructions from the control store, separates the control field bits, and sends them to other areas of the processor for execution. In addition the Sequencer:

   1. Controls microprogram flow by executing conditional microinstructions branches

   2. Contains logic for the Environment Register Condition code bits

   3. Produces SYNCA and SYNCB pulses to aid in processor troubleshooting.

b. The Writable Control Store arrays contain microprograms that define the macro instruction set and microdiagnostics. The control store is located in high-speed static RAMs, which are loaded from an external disc or tape drive. The initial bootstrap microcode is loaded from the DDT PROMs located on the CC board. At present users cannot write their own microcode into the control store.

Figure 3-2 shows the SQ board interconnections, functional units, major circuits, and related processor status screen errors.

3.1.3 Channel and Control Board (CC)

The following functional units are located on the CC board:

a. The I/O Channel is a single-burst multiplexed communication channel through which all I/O operations take place. The I/O Channel provides the interface between the NonStop TXP processor and device-dependent I/O controllers and, in conjunction with the CPU microcode, recognizes the EIO, reconnect, IIO, HIIO, the cold load channel command sequences, and the request signals from the I/O controllers (RCI, LIRQ, and HIRQ).

b. The Diagnostic and Data Transceiver (DDT) provides a communications link to the Operations and Service Processor (OSP) and CPUs. The OSP may be connected locally or remotely through a modem. The Processor Maintenance Interface (PMI) patch panel provides fan-out/fan-in between the DDTs of all processors located within the entire system and the OSP and modem. The PMI provides disabling hardware to maintain the security of processors against unauthorized or unintentional access through the DDTs.

The DDT provides the following specific functions:

1. Initialization of the processor at power-on or RESET by performing internal checks, which include checksumming PROMs, scan logic tests, PMI interface turnaround test, and other internal tests.

2. Fault Isolation.

3. An XRAY timer to measure system performance.

4. Communication between the OSP and a CPU in a HALT state through the PMI interface. This permits the transmission of the processor status information to the OSP upon operator request.

5. Remote RESET of the selected processor on command from the OSP. (Switches on the PMI are provided to prevent accidental or unauthorized resetting of processors).

6. Remote HALT of the selected processor from the OSP or CPU by means of a software interrupt. (This function is controlled by a switch located on the PMI to prevent accidental or unauthorized HALTing of CPUs).

7. Remote starting of the HALTed processor on command from the OSP. (This command does not restart processors that have been HALTed singly; thus, there are two types of HALT states).

c. The Interval Timer provides the CPU with a 10 ms interrupt to run the message system and keep the time of day.

d. The Special ALU (SALU) allows logical and arithmetic operations to be overlapped between the SALU and the Main ALU located on the IP board.

e. The Multiply and Divide steps use the SALU to provide a one bit per step multiplication and division.

f. The Scratch Pad Registers provide the microprogrammer sixteen sets of 256 registers for general use.

Figure 3-2 shows the CC board interconnections, functional units, and related processor status screen errors.

3.1.4 Memory Control Board (MC)

The following functional units are located on the MC board:

a. The Memory Control Unit is the interface between the CPU and main memory. It contains the processor clock generation logic and also controls the REFRESHing of the dynamic memories used on the Memory Array Boards (MM). The MCU also performs diagnostic functions.

b. The Interprocessor Bus (IPB) circuitry sends and receives 16-word packets.

c. System Clock: The clock generator provides clocking for the entire processor, with the exception of the interprocessor bus, which is clocked by the bus controller. Six clock lines carry the clock signals to all of the subsystems. Each board in the system is clocked from the MC board.

d. The Barrel Shifter performs single-bit and mutli-bit shifts and rotates for single and extended word lengths. This operation is pipelined so that the result of the current operation is stored in an internal register, while the result of the previous operation is returned on the special data path (SMBUS).

e. The Interrupt Logic circuitry permits the orderly transfer of CPU control from an executing program either to a micro code routine or to one of several operating system routines known as interrupt handlers.

Figure 3-2 shows the MC board interconnections, functional units, and related processor status screen errors.

3.1.5 Memory Array Board (MM)

The following functional units are located on the MM board:

a. The Memory Array (RAM Array) stores the instructions and operands used by the processor. It maintains 1024K 22-bit words of data storage. It accepts write data one word at a time and can buffer for one-, two-, three-, or four-word block writes. Data is read in four-word blocks and returned one word at a time.

b. The Memory Data Register (MD Register) holds four words of data either to be written to, or read from, the Data Store RAMs.

c. The NOVRAMs determine memory address configurations.

Figure 3-2 shows the MM board interconnections, functional units, and related processor status screen errors.

The processor uninterruptable supply of +5 volts is used to REFRESH the dynamic RAMs under control of the Memory Control Unit should main power be lost.

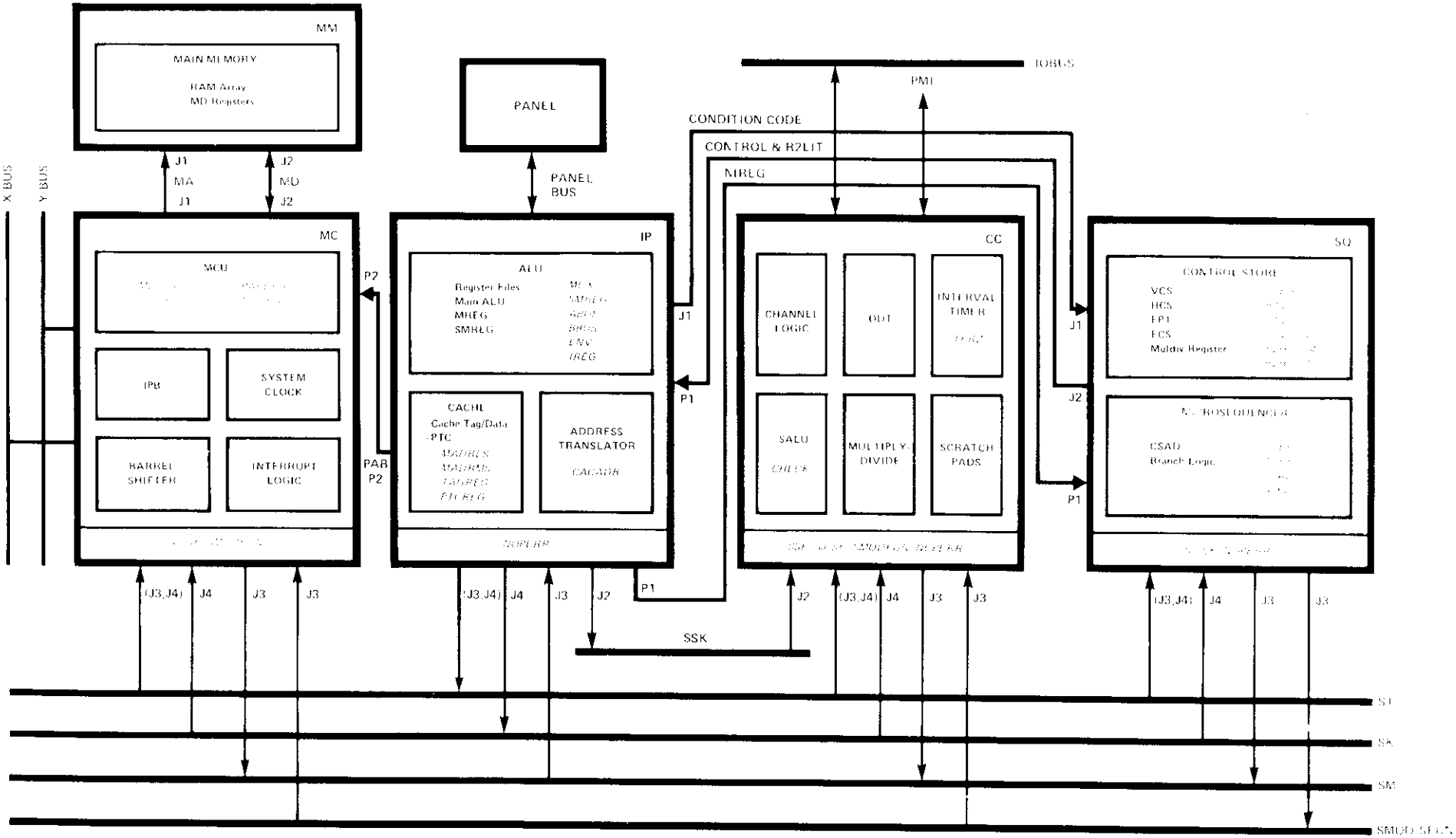


Figure 3-2 NonStop TXP Processor Functional Block Diagram

SECTION 4
INSTALLATION

4.0 INSTALLATION

The revision level of the upper and lower processor backplane determines the correct procedure for installation of a NonStop TXP CPU. Revision-A (upper and lower) backplanes require modification. Revision-B (upper and lower) backplanes do not require modification.

NOTE

The revision level is printed in the upper left hand corner of the backplane.

Figures 4-4 through 4-8 at the end of this section are charts that summarize the entire installation procedure.

4.1 REVISION-A UPPER AND LOWER PROCESSOR BACKPLANE

If the processor cabinet at the installation site has a Revision-A backplane, the backplane must be modified at the slots for the MM, IP, and CC boards.

Figure 4-4 is a chart that summarizes the backplane modification procedure.

Proceed as follows:

a. At the MM boards slots, install jumpers (wirewrap) on the following pins (see Figure 4-1):

MM slots (1, 9, 17, 25)---No Jumpers required.

MM slots (2, 10, 18, 26)--Pin #1 jumpered to Pin #41.

MM slots (3, 11, 19, 27)--Pin #1 jumpered to Pin #42.

MM slots (4, 12, 20, 28)--Pin #1 jumpered to Pins #41 and #42

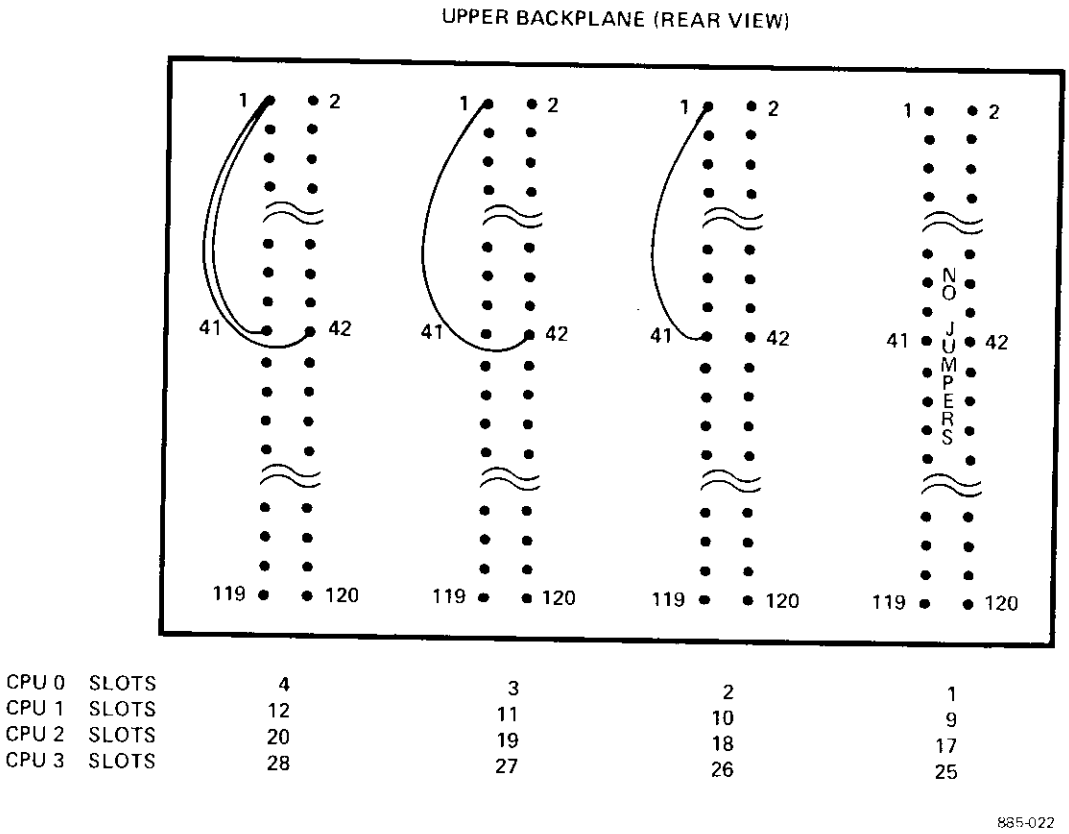


Figure 4-1 Memory Board Slot Assignment Jumpers

b. Modify the lower backplane at the IP board slots as follows:

   1. Remove the Control Panel cable (P2) from the IP board backplane.

   2. Cut off backplane P2-pins 65 through 70 (see Figure 4-2).

   3. Replace Control Panel cable.

c. Modify the lower backplane at the CC board slots as follows:

   1. Remove the PMI cable (P2) from the CC board backplane.

   2. Cut off backplane P2-pins 73 through 80 (see Figure 4-2).

   3. Replace PMI cable.

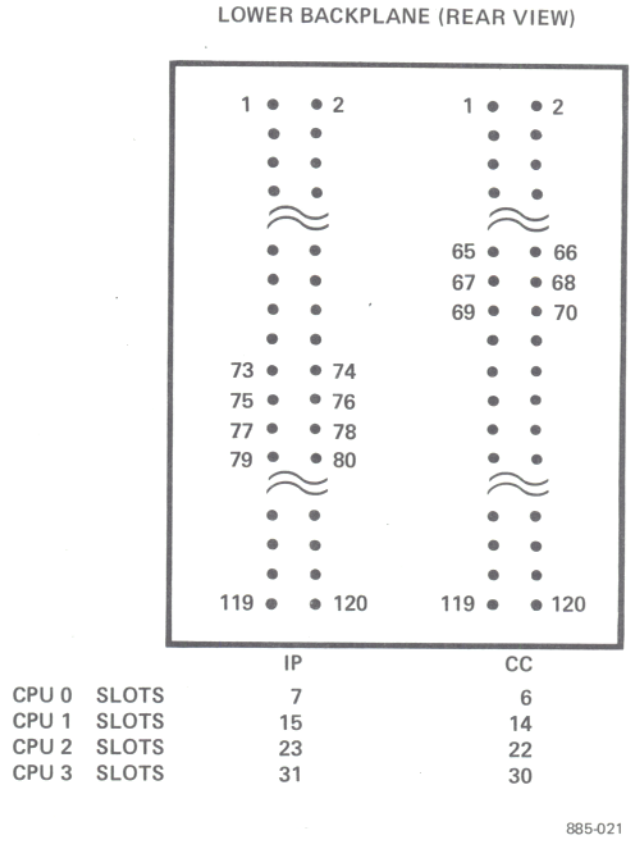


Figure 4-2 IP and CC Boards Pin Cuts

d. Install all NonStop TXP CPU boards using the board replacement procedure described in Figure 5-4.

4.2 INSTALLING A NonStop TXP CPU IN A NonStop II SYSTEM

To add a NonStop TXP CPU to a NonStop II system, perform the following:

a. Determine whether extra I/O power is needed for the new configuration. (Three I/O-only power supplies are required for a NonStop II/NonStop TXP mixed system.)

b. Complete the horizontal bus V-tab requirements on a System Cabinet Layout Form (Part Number 82979). Figure 4-3 shows a sample form with processor layout and calculation entries.

c. Modify the Horizontal bus and Plenum Diode as follows:

1. Power down all I/O-only and processor power supplies. Disconnect the processor power supplies and remove them from the cabinet.

2. Identify the Processor power supply slot for the NonStop TXP CPU and replace the old plenum diode assembly with a new plenum diode assembly (Part Number 59790).

3. On the Horizontal bus, remove all 5-inch wires attached to even-numbered V-tabs and I/O backplane.

NOTE

Even-numbered V-tabs (Processor power supplies) are not to be used to power I/O controller boards. Only the IPB/PMI regulator power connections will be used by the even-numbered V-tabs (V2 and V4).

4. Install 12-inch wires to I/O backplane and connect to odd-numbered V-tabs. See Figure 4-3 for correct odd-numbered V-tab connections.

Figure 4-5 is a chart that summarizes the bus bar and plenum diode modification procedure.

PROCESSOR CABINET (REAR)

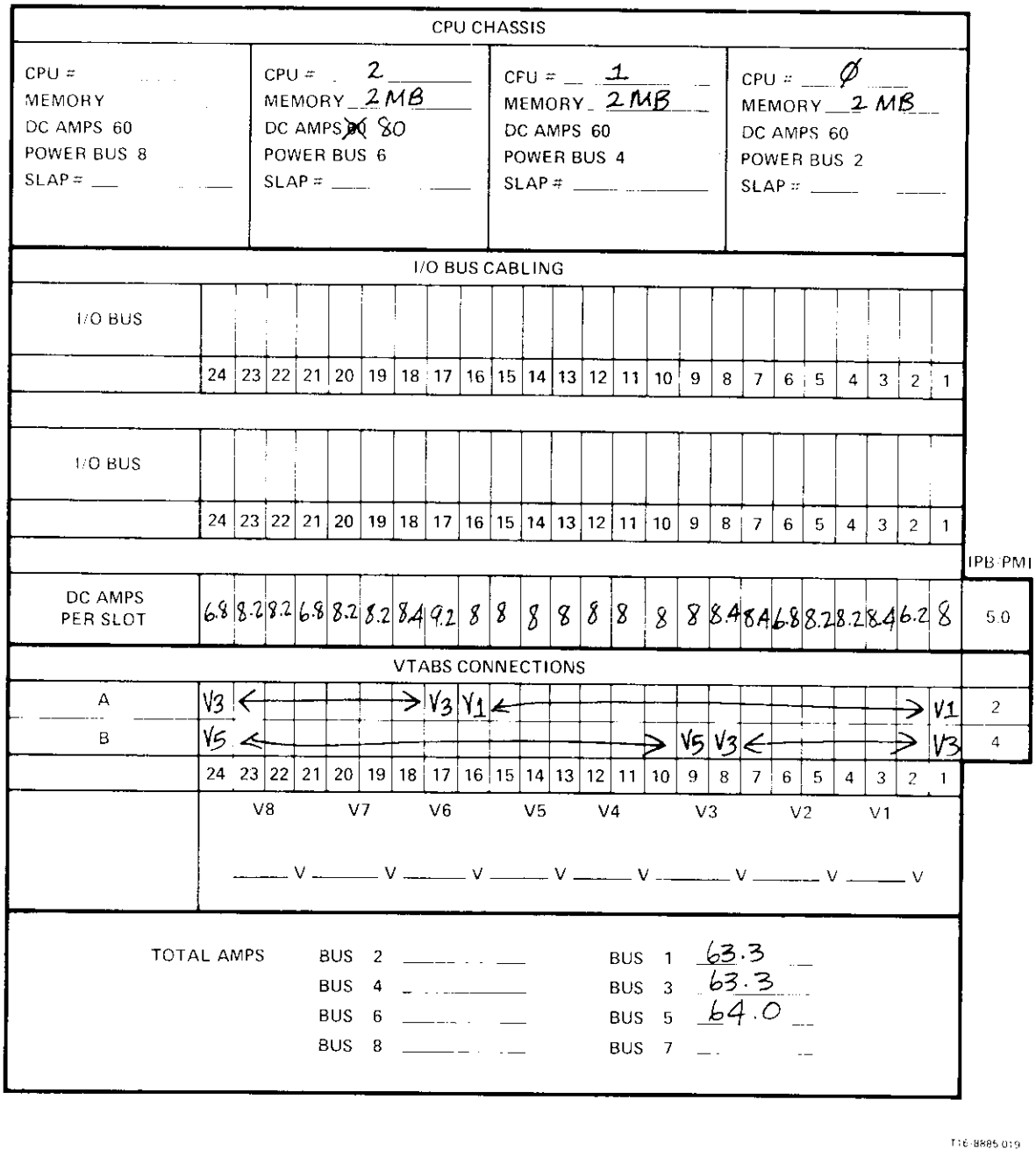


Figure 4-3 Sample System Cabinet Layout Form (Back)

d. Adjust all power supplies as follows:

**** CPU SUPPLIES ****

1. 5V IPS-----Adjust the 5-volt IPS while measuring the voltage on the vertical bus bar. The voltmeter should be connected to the bus at the point where it connects to the PROCESSOR LOWER backplane. The 5-volt IPS is labeled "5I" and the voltmeter return should be connected to the point labeled "G1". Adjust to 5.05 (+ .01).

2. 5V UPS-----Adjust the 5-volt UPS while measuring the voltage on the vertical bus bar. The voltmeter should be connected to the bus at the point where it connects to the PROCESSOR LOWER backplane. The 5-volt UPS is labeled "5U" and the voltmeter return should be connected to the point labeled "G2". Adjust to 5.05 (± .01).

3. 12VMEM-----Adjust the 12-volt (SEMI MEM) while measuring the voltage on the vertical bus bar. The voltmeter should be connected to the bus at the point where it connects to the PROCESSOR LOWER backplane. The 12-volt memory supply is labeled "VM" and the voltmeter return should be connected to the point labeled "G2". Adjust to 12.05 (± .01).

**** I/O-ONLY SUPPLIES ****

4. Adjust the I/O-only supplies to 5.7 (± .10) volts. This measurement is to be made at the horizontal bus bar using the correct V-tab. The ground return for the voltmeter should be connected to one of the ground return V-tabs located on the horizontal bus bar.

5. Measure the output of the I/O power regulators at pin 120 of each I/O controller card. The output should read 5.05 (+ .02) volts. If adjustment is necessary, adjust the BOTTOM pot on the I/O regulator card. (The TOP pot is for current limit and is to be adjusted at the factory ONLY). The ground return for the voltmeter should be connected to one of the ground return V-tabs on the horizontal bus bar.

NOTE

After all modifications have been made to the backplanes, horizontal bus bar, plenum diodes, and the power supplies have been adjusted, the processor cabinet is compatible with both NonStop II and NonStop TXP processors.

Figure 4-6 is a chart that summarizes the power supplies adjustment procedure.

4.3 INSTALLING A NEW NONSTOP TXP SMP BOARD IN THE OSP.

The OSP SMP board must be replaced with a new SMP board (Part Number 42540) in order to run diagnostics on the NonStop TXP CPUs. Figure 4-7 summarizes the procedure.

4.4 DIAGNOSTICS FOR THE NonStop TXP CPU AND OSP SMP BOARD

Run the following OSP and NonStop TXP diagnostics:

a. At power-up, OSP Self tests will indicate pass or fail of the SMP board. Refer to OSP Maintenance Manual for complete testing information.

b. TXP Processor General Test Diagnostic (CPU1432) and Memory Test Diagnostic (MEM2432). Refer to paragraph 5.1.3 this manual for additional information on diagnostics.

Figure 4-8 summarizes this procedure.

Refer to Section 5 (Corrective Maintenance) for any corrective action or installation and removal procedures of CPU boards.

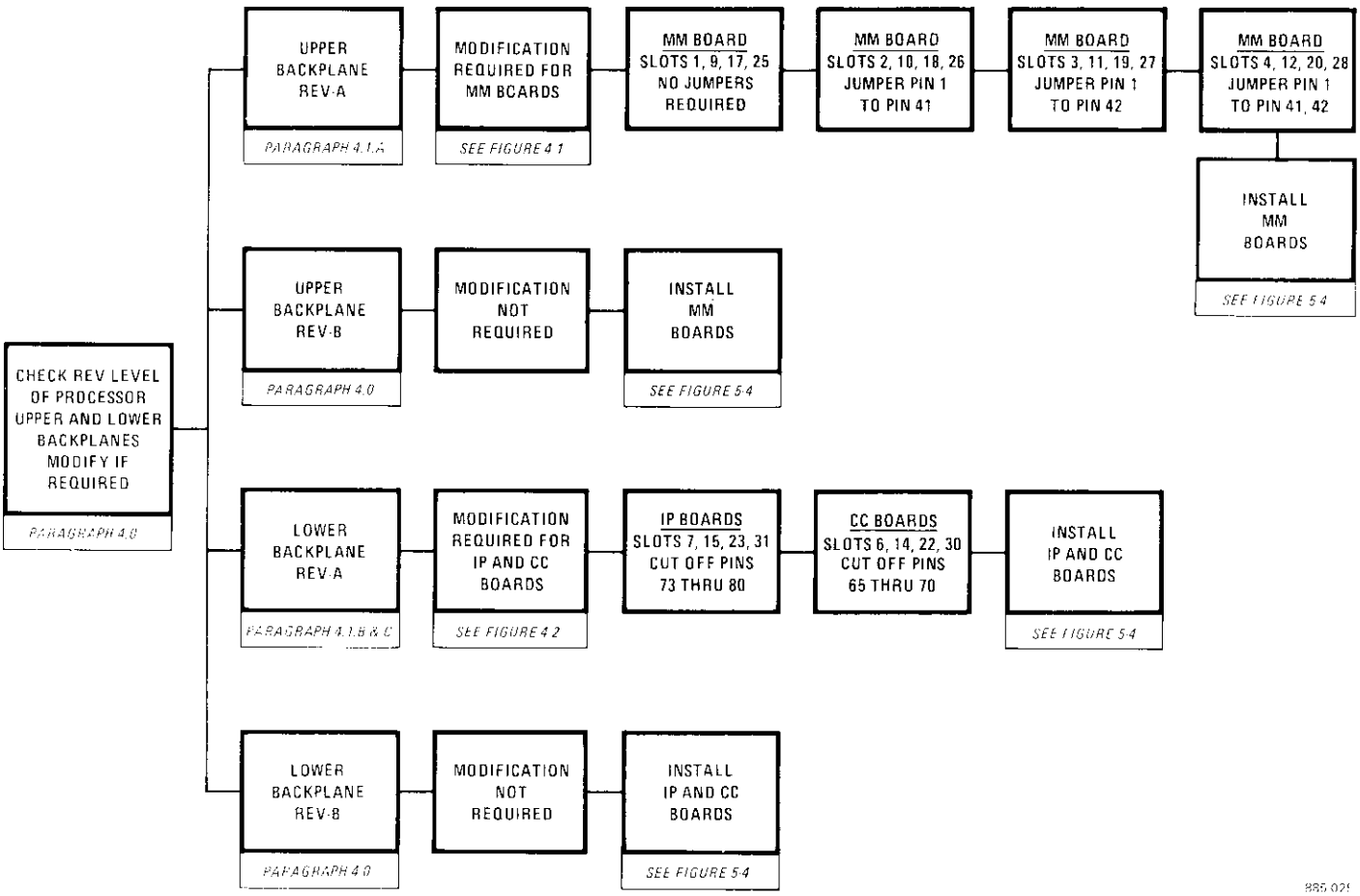


Figure 4-4 Processor Backplane Revision Level and Modification Chart

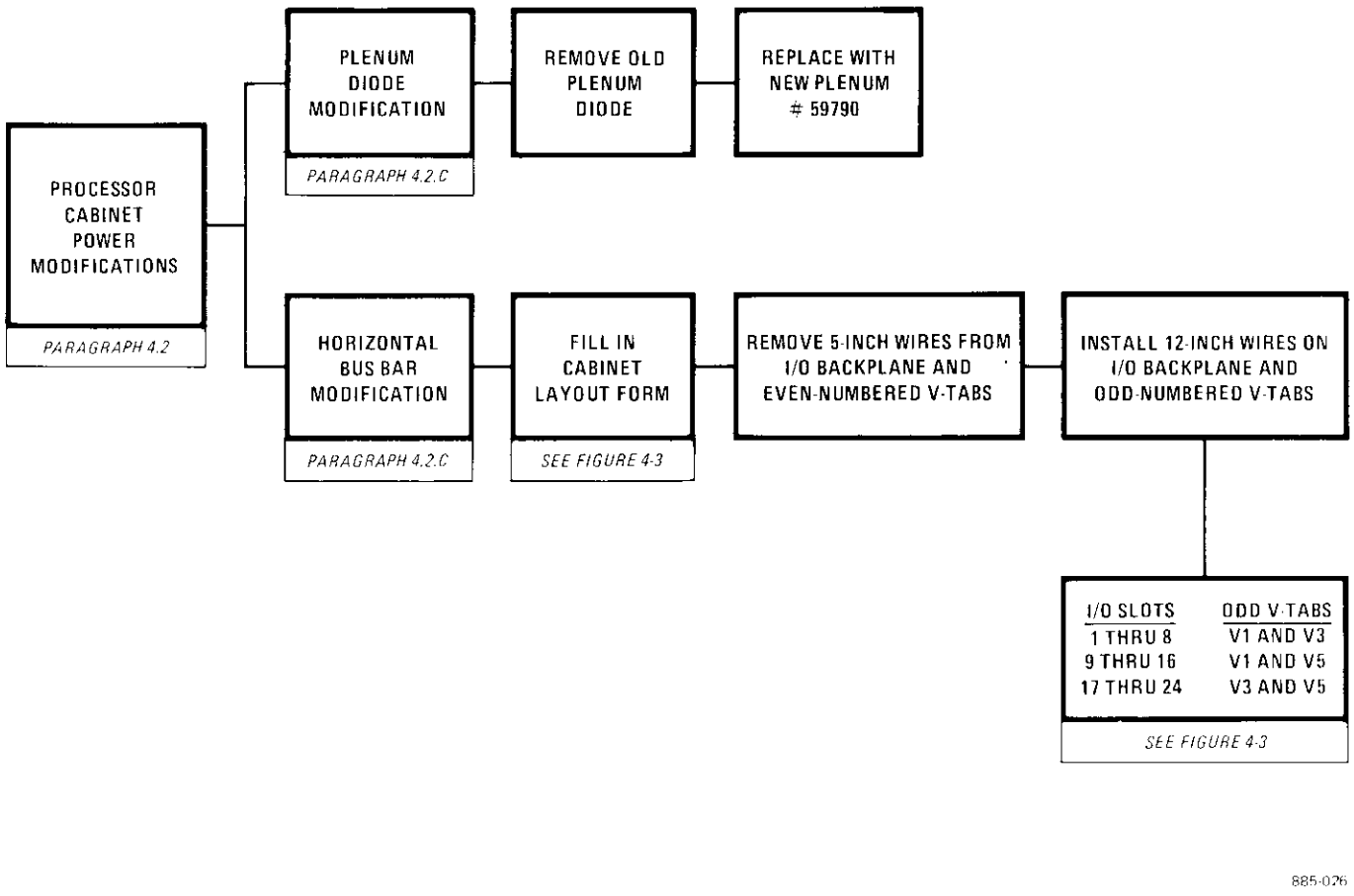


Figure 4-5 Plenum Diode and Horizontal Bus Bar Modification Chart

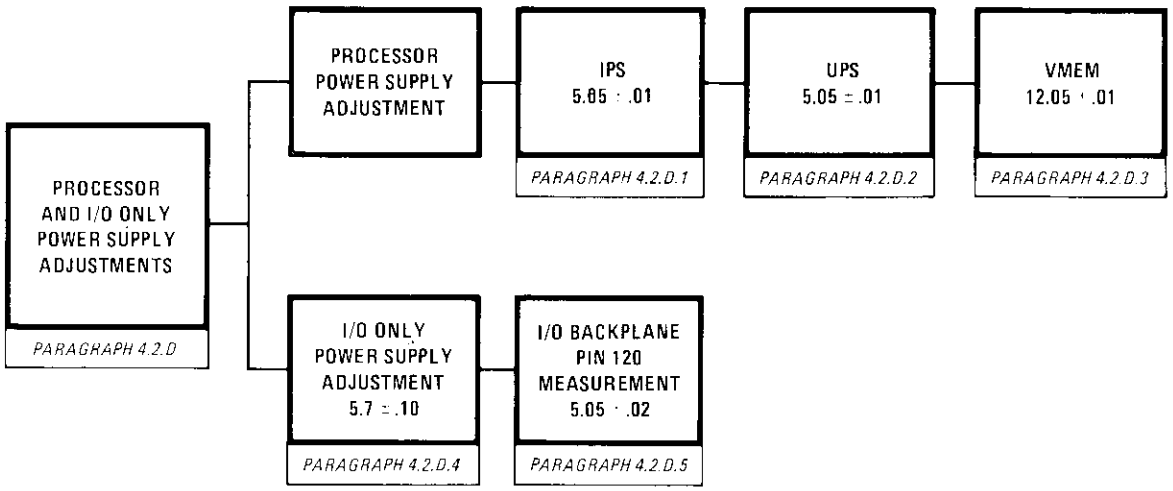


Figure 4-6 Processor and I/O-Only Power Supply Adjustment Chart

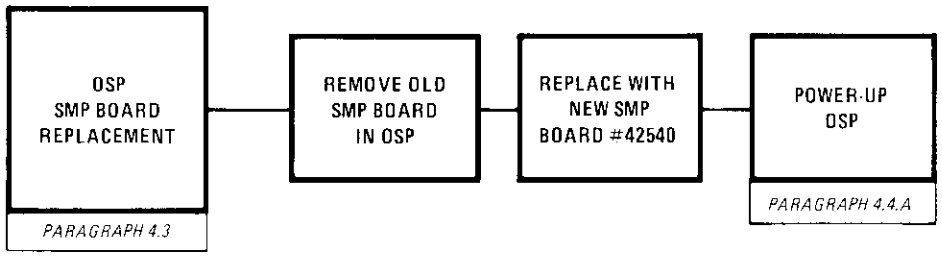


Figure 4-7 OSP SMP Board Installation Chart

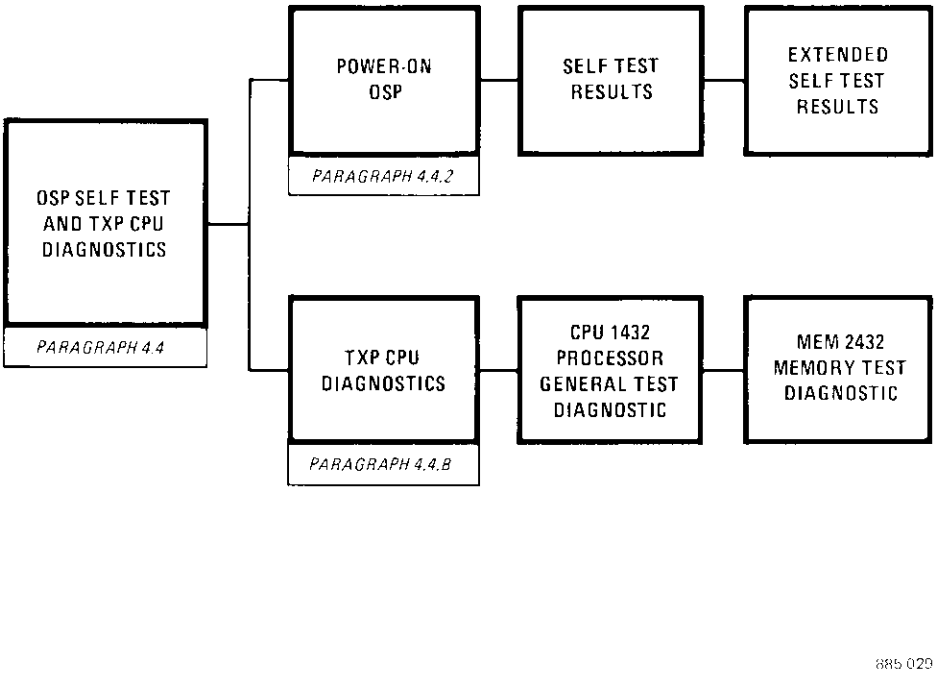


Figure 4-8 OSP Self Test and NonStop TXP CPU Diagnostic Chart

SECTION 5
CORRECTIVE MAINTENANCE

5.0 CORRECTIVE MAINTENANCE

Field repair of the NonStop TXP processor is accomplished by replacing defective CPU boards. All defective TXP boards are sent to the Customer Engineering Headquarters for disposition. (Refer to paragraphs 5.5 and 5.6 for the mailing location, packaging, and shipping instructions.)

The primary maintenance objective in correcting a processor failure is to take the necessary corrective action without affecting the entire system. To ensure this, the suggested maintenance approach is as follows:

a. Ensure that user application programs remain operational during the period of maintenance. In cases where a processor is rendered inoperable:

   1. All I/O controllers owned by the failed processor are taken over automatically by other operational processors. This is assuming that switching is automatic. However, manually using PUP primary commands will ensure switching to other operational processors.

   2. NonStop processes are automatically switched to their respective back-up processes in other operational processors.

b. Have the system manager take off line only that portion of the system necessary to perform maintenance.

c. Record the processor failure information from the appropriate Processor Status Screen and the Status Code from the DDT lights.

d. Run diagnostic programs to localize problems and then take the appropriate corrective action.

e. Have the system manager restore the system to the original configuration and level of performance by restarting any applications that were rendered inoperable due to the failure, and verifying the integrity of any disc volumes that may have been damaged as a result of the failure.

5.1 TROUBLESHOOTING

Troubleshooting processor failures is done by analyzing the CC board status indicator lights, processor and system status screens on the OSP, and control panel lights. Often the information provided by these messages is adequate for localizing board failures within the processor subsystem. Failures not readily defined may require the use of diagnostic programs described in paragraph 5.1.3.

5.1.1 CC Board Status Indicators

The location of the four indicator lights on the CC board is shown in Figure 2-2, and the location of the board within the processor subsystem in Figure 2-1.

As part of its power up program, the Data and Diagnostic Transceiver (DDT), located on the CC board, performs basic processor tests. The failure of a specific test is registered as an error code on the four indicator lights.

Table 5.1 lists in numerical order all possible combinations of indicator codes along with suggested corrective actions. (Refer to paragraph 5.1.2.2 for a description of DDT detected errors as displayed by the OSP).

NOTE

The most significant bit (MSB) is light number 1 located on the top of the display, and the least significant bit (LSB) is represented by light number 4 on the bottom.

Table 5.1 CC Board Indicators

INDICATORS MSB----LSB 1 2 3 4	OUTPUT DESCRIPTION
0 0 0 0	NO POWER. Check power to the processor.
0 0 0 1	CHECKSUM PROM 0. Replace the CC board.
0 0 1 0	UART CHECK. Replace the CC board.
0 0 1 1	PMI TURNAROUND CHECK. Check the data path from the DDT to the PMI.
0 1 0 0	CHECKSUM PROM 3 or 4 bad. Replace the CC board.
0 1 0 1	SCAN STRING CHECK. Check the processor status screen for scan failures.
0 1 1 0	CPU CLOCK CHECK. Replace CC board first, then the SQ board.
0 1 1 1	CTC CHECK. Replace CC board.
1 0 0 0	DDT RAM CHECK. Replace CC board.
1 0 0 1	DDT OK. Normal Operation State.
1 0 1 0	MEMORY CONFIGURATION CHECK. Verify that the memory slot assignment jumpers on the backplane are correct. Using the (F3) Configuration screen, validate the configuration. Check the processor status screen for DDT detected error information. (Paragraph 5.1.2.2.)
1 0 1 1	BOOT LOAD. In sequence, replace the SQ, CC, and the IP board. If the error condition remains, change the cables.
1 1 0 0	SCAN CONTROL CHECK FAILED. Replace the CC board.
1 1 0 1	VCS LOAD FAILED. In sequence, replace the SQ and CC boards. If the error condition remains, change the cable.
1 1 1 0	RAM PARITY ERROR. Replace the CC board.
1 1 1 1	RESET. RESET is currently being asserted.

These tests, listed in sequence of execution, function as follows:

a. RESET/POWER ON ASSERTED (1111). This is executed when RESET is applied through either the OSP or front panel reset switch. The power light on the front panel is off while RESET is being asserted.

b. TEST FOR DDT DOUBLE-BIT ERRORS (1000). A series of ones and zeros are walked through the DDT RAMs. If an error is registered, the program goes to the RAM initialize loop and leaves error code 1000 on the indicators.

c. CHECKSUM PROM 0 (0001). This code appears when the checksum program stops after unsuccessfully attempting to access a non-existent PROM (ensure that PROMs P0, P3, P4 are installed, not all PROM slots are used) or when PROM 0 fails.

d. UART TEST (0010). UART failure. (A UART failure will not inhibit coldloading the processor or cause the DDT to stop.)

e. PMI TURNAROUND TEST (0011). The PMI communication and data integrity are checked. (A failure at this point will not inhibit coldloading the processor.) After coldloading has occurred, and no other tests fail, the DDT will leave 0011 on the indicators. (Check the path from the DDT board to the PMI.)

f. CTC CHECK (0111). The Counter Timer Chip (CTC) is set to interrupt, then it is checked to see if the interrupt has occurred. The CTC must be functional to perform the microload; if it is not, the 0111 code remains on the indicators.

g. CHECKSUM OF PROMs 3 AND 4 (0100). PROMs 3 and 4 contain the microcode that must be checked before executing the code. If a failure is detected, 0100 remains on the indicators.

h. SCAN COUNTER CONTROL CHECK (1100). The scan counter and the scan paths to the interfaces are checked. If a failure occurs, 1100 is left on the indicators. (This test is only on the CC board.)

i. SCAN STRING CHECK (0101). The DDT scans a data string into the processor. The data is then scanned out and compared to the original data. An error in the comparison of data causes code 0101 to remain on the indicators and reports the failed string to the OSP Status Screen (refer to paragraph 5.1.2.2). Corrective action is determined by using the OSP to isolate the board that failed.

j. CPU CLOCK CHECK (0110). The CPU clock is checked by placing a value of 0000 in the Control Store Program Counter (CSPC). The RESET state is then scanned in and causes the CPU Clock to increment. Failure to increment will cause code 0110 to remain on the indicators.

k. BOOT LOAD (1011). Loading of the initial Boot-code into control store of the SQ board. The sequence of events for preparing the processor during BOOT LOAD are as follows:

1. Load Scan String into the microloader:

   a) Scan data into HCS Register

   b) Scan in "write HCS" Command

   c) Issue clocks

   d) Loop until all of HCS is written

   e) Scan data into VCS Register

   f) Scan in "write VCS" Command

   g) Issue clocks

   h) Loop until all of the VCS is written.

2. Start-up microloader (freezes off):

   The microloader then writes the HCS by taking data from the Receiver Character Buffer, moving it to the HCS Register through the MULDIV, then writing HCS using microcode operations.

3. Turn on freezes (1101):

   The microloader writes the VCS by taking data from the RCB, moving it into the VCS Register, then writing the VCS using microcode operations.

   If this algorithm fails, a 1101 is registered on the CC board indicators. When this occurs, the front panel lights will indicate the source of error. Initially, the DDT writes 1110000000000111 on the front panel lights. The microloader, however, will write all zeros to the front panel lights.

l. MEMORY CONFIGURATION CHECK (1010). The NOVRAMs on the MM board are read and memory configuration is checked. If more than one string responds at a time, or if the board serial number and its complement do not match, the operation halts with a code 1010 on the indicator lights. Since string selection tests are also performed at this time, they may identify a board that is responding to more than one memory address. Refer to paragraph 5.1.2, for more information on the OSP Screen Error Messages.

m. INITIALIZE CTC START UP PROCEDURE (0111). The CTC is initialized to prepare the DDT for normal interrupt operation.

n. DDT OK (1001). Normal Operation State.

5.1.2 OSP Screen Error Messages

More information may be obtained from a CC board's Diagnostic and Data Transceiver (DDT) by using the Operations and Service Processor (OSP). The OSP, along with the Processor Maintenance Interface (PMI), enables the operator to get status information from any CPU or all CPUs within a system without interfering with the system's operation.
The following troubleshooting information highlights the use of the OSP as a system maintenance terminal.

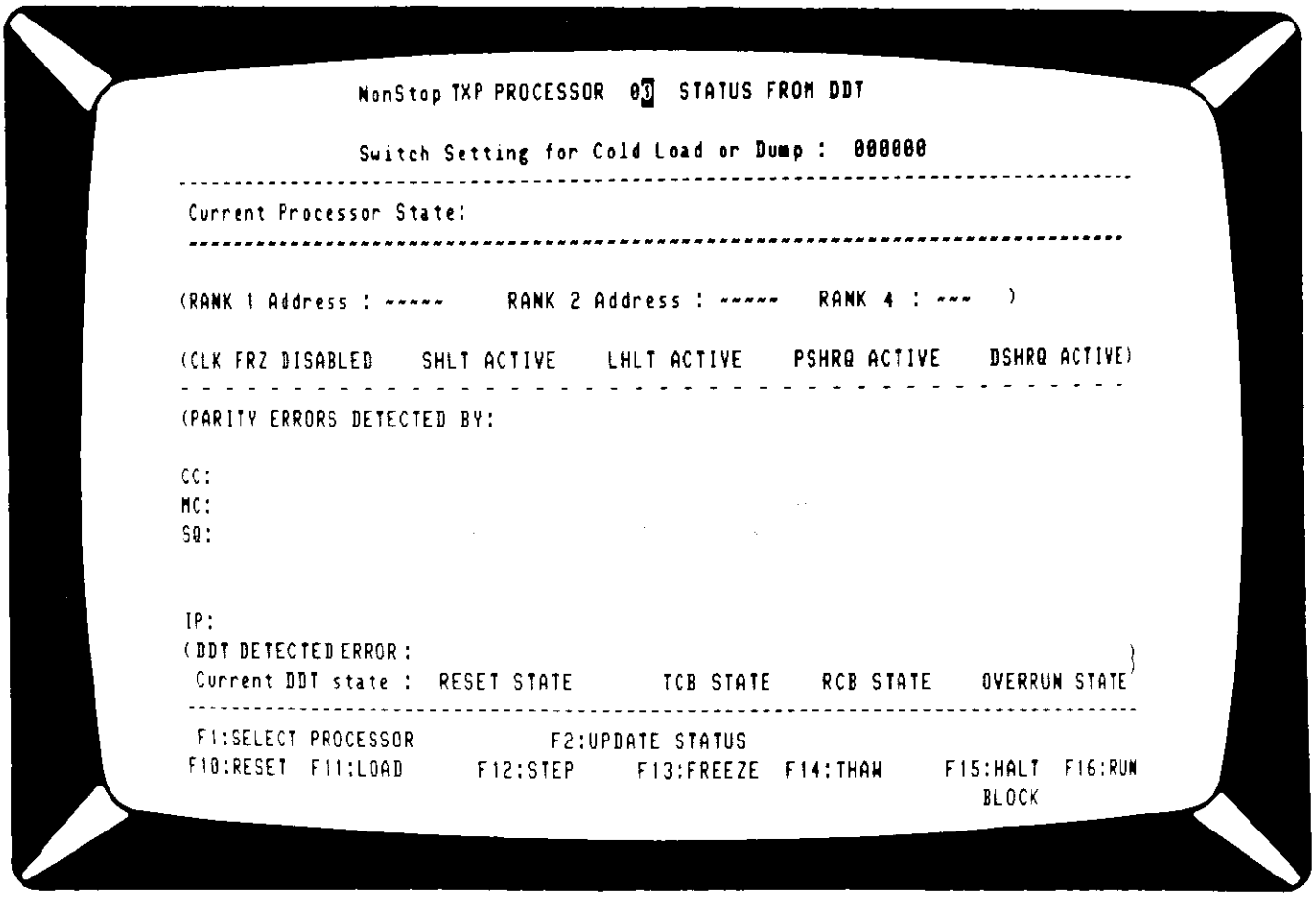
Screen error messages are called up on the OSP by depressing a shifted F6 from the OSP. The processor then can be selected, and its status displayed. Refer to Table 5.2 for a description of function modes and their operation.

Table 5.2 OSP Function Modes

KEY	FUNCTION MODE	OPERATION
Shifted F1	Conversational Terminal # 1	Runs a conversational-mode Command Interpreter.
Shifted F5	System Status Screen	Displays a summary of status for all processors in the system.
Shifted F6	Processor Status Screen	Displays a status report on a selected processor.

Since the information comes from the DDT, the remainder of the processor's operation is unaffected. The Processor Status Screen displays the basic processor state (running, idle, or frozen) along with other conditions. Exceptional states are indicated only if they exist at the time the processor status was fetched.

Figure 5-1 and the following descriptions explain the messages that can occur on a NonStop TXP Processor Status Screen. These messages represent conditional states of the processor that are displayed only if the conditional state is true.



885-024*

Figure 5-1 NonStop TXP Processor Status Screen

5.1.2.1 Parity Errors Detected By: (Conditional)

This field lists both the points in the processor where parity errors were detected and each board detecting an error. It does not attempt to diagnose the source of the error. If there are no errors, the entire field is blank. For example, if the OSP detected all parity errors at once, the parity error field would appear as follows:

```
PARITY ERRORS DETECTED BY:

CC:  SJ SK  SMODFUN NOPERR  SSKBUS  CHECK  ITFRZ
MC:  SJ SK  SMODFUN          MDIAG   OPCHK  PABERR  MCUBAD
SQ:  SJ SK  TCHECK  NOPERR  CCERR     CSAD      NIREG
                            R1VCS_01  R2VCS_23  R1VCS_4  R2HCS_04
                            R2HCS_79  R3ERR
IP:  ABUS    BBUS   NOPERR  ENV  IREG  MADRLS  MUX  TAGREG  MADRMS
                            PTCREG  SMREG  CACADR
```

Description of reported errors in the Parity Errors Detected Field:

Board	Parity Error	*Failing Board	Description
CC	SJ	CC	Parity error detected on the SJ bus. Each board detecting the error reports a parity error. The SJ bus is routed through the J3 and J4 front edge connectors. If this error is indicated by all three boards at the same time, the IP board is probably causing the error. If the error remains after board replacement, check cables.
MC	SJ	MC	
SQ	SJ	SQ	
CC,MC,SQ	SJ	IP	
CC	SK	CC	Parity error detected on the SK bus. Each board detecting the error reports a parity error. The SK bus is routed through the J4 front edge connector. If this error is indicated by all three boards at the same time, the IP board is probably causing the error. Cable J4 may also be defective.
MC	SK	MC	
SQ	SK	SQ	
CC,MC,SQ	SK	IP	
CC	SMODFUN	CC	Parity error detected on the SMODule and SFUNction buses. Each board detecting the error reports a parity error. The buses are routed through the J3 front edge connector. Should this error be caused by a control store error, a R2HCS_79 error also occurs.
MC	SMODFUN	MC	

* When more than one board has been listed for a specific error condition, the most probable board is listed first with the next probable board following.

Board	Parity Error	Failing Board	Description
CC SQ IP	NOPERR	CC SQ IP	Parity error detected as a result of testing the NOP and NOP* signals and finding them equivalent.
IP IP	ABUS BBUS	IP IP	Parity error detected on data being input to the ALU on the IP board. An ABUS error corresponds to the A side of the ALU. This error is probably local to the IP board.
IP	ENV	IP SQ	Parity error detected on the ENVironment register. This error is probably local to the IP board.
IP	IREG	IP	Parity error detected on the Instruction REGister. This error is probably local to the IP board.
IP	MADRLS	IP MC	Parity error detected on the Memory Address Least Significant register. This error is probably local to the IP board. This can occur along with a PABERR (MC board).
IP	MUX	IP SQ	Parity error detected by the IP board. The ABUS, BBUS, SJBUS, SKBUS mux selected are sent from the SQ to the IP board along with a parity bit that detected the error. These signals are routed through the J2 front edge connector. R2HCS_04 is also asserted if this an SQ problem.
IP	TAGREG	IP	Parity error detected by the cache TAG REGister. This error is probably local to the IP board and is possibly caused by a TAG store RAM error.
IP	MADRMS	IP	Parity error detected on the Memory Address Most Significant register. This error is probably local to the IP board.
IP	PTCREG	IP MC	Parity error detected by the Page Table Cache REGister. This error is probably local to the IP board and may be caused by a PTC RAM error, this may occur along with a PABERR (MC board).

Board	Parity Error	Failing Board	Description
IP	SMREG	(See list)	Parity error detected on the SMBUS. This bus receives data from the other processor boards, and is routed through the J3 front edge connector. Faults may be localized by examining the R4REG, which reports the R4 SMOD that placed the data in error on the SMBUS. If the board indicated by R4 SMOD list is replaced and the problem still exists, replace the IP board.

→

R4 SMOD	Replace FRU
%00	CC
%01	CC
%02	MC
%03	MC
%04	MC
%05	MC
%06	SQ
%07	SQ
%10	CC
%11	CC
%12	CC
%13	CC
%14	CC
%15	CC
%16	CC
%17	SQ

NOTE

Because Rank 1 and Rank 2 addresses are obtained by reading the appropriate scan string, which entails stopping the clocks, the addresses are not displayed when the processor is running; they are displayed only when the processor is halted or frozen. RANK 4 is displayed only when a SMREG Parity Error occurs.

IP	CACADR	IP SQ	Parity error detected as the CAC and ADR fields are transmitted from the SQ board to the IP board over the J1 front cable. If this fault is caused by the SQ board, the R2HCS_79 error also occurs.

Board	Parity Error	Failing Board	Description
CC	SSKBUS	IP CC	Parity error detected on the SSKBUS. This is a private copy of the SKBUS used by the Scratch Pad registers for addressing. This bus uses the J2 front edge connector.
CC	CHECK	IP CC	This error is caused by an internal microcode self-checking error. The CHECK microoperation found an error condition that caused the freeze. The fault depends on the specific test being performed, but the IP or CC is probably at fault. Recording the R1 and R2 addresses is useful in analyzing the error.
CC	ITFRZ	CC	Error detected by the interval timer logic.
MC	MDIAG	MC	Parity error detected on the MDIAG register. This register is a control register used by the processor diagnostics to alter certain processor operations during testing. This register is local to the MC board although it is loaded by way of SJBUS data and may occur along with a SJ Bus Error.
MC	OPCHK	MC MM	Error detected as a result of a miscompare between the OPCHK state machine on the MC board and the OPCHK machine on the selected MM board. This indicates a synchronization problem between the Memory Control Unit and the selected Memory Board. This error can be caused by an error in initialization, possibly because of a NOVRAM failure on an MM board.
MC	PABERR	MC IP	Parity error detected on the physical address as sent from the IP board to the MC board. This is the physical address to be used by the memory logic for memory access. The physical address is transmitted over the P1 and P2 backplane connectors. PABERR may occur along with a MADRLS or PTCREG error.
MC	MCUBAD	MC	This error is caused by an invalid state detected within the MCU state machines. The error is local to the MC board Memory Control Unit.

Board	Parity Error	Failing Board	Description
SQ	TCHECK	SQ	This error is caused by an internal microcode self-checking error. The TCHECK microoperation found an error condition that caused the freeze. The fault depends on the specific test being performed, but the SQ is probably at fault. Recording the R1 and R2 addresses is useful in analyzing the error.
SQ	CCERR	SQ IP	Error detected in the Condition Code logic as the data flows between the SQ and IP through the J1 front edge connector.
SQ	CSAD	SQ	Error detected in the addressing of control store. The error is local to the SQ board.
SQ	NIREG	IP SQ	Parity error detected by the SQ board. The SQ contents of the NIREG (next instruction) is sent from the IP to the SQ over the P1 backplane connector.
SQ SQ SQ SQ SQ SQ	R1VCS_01 R2VCS_23 R1VCS_4 R2HCS_04 R2HCS_79 R3ERR_	SQ SQ SQ SQ SQ SQ	Parity error detected in control store by the control store parity checkers. As microinstructions are read from control store RAM, the data is checked against stored parity data. This error is local to the SQ board control store section. Any of these errors is likely to cause one or more other errors.

5.1.2.2 DDT Detected Errors

The DDT Detected Error field displays internal processor errors as detected by the DDT. Although multiple error conditions are reported to the OSP, the OSP can display only one error message at a time. The first error reported is displayed; subsequent errors appear on the Processor Status Screen only when preceding errors are corrected. The following conditions may be displayed in this field:

Failed Board	Error Message	Description
CC	CHECKSUM IN PROM 0	This condition occurs when attempting to access a non-existent PROM (ensure that all PROMs are installed) or when PROM 0 fails.
SQ, CC	MICROCODE LOAD	The DDT timed out while sending data across to the processor. If an error freeze appears, check the SQ board. If there is no error freeze, check the CC board.
SQ, CC	EPT CHECKSUM	The checksum returned to the DDT from the microcode is in error.
CC	CHECKSUM in PROM 3	Bad PROM on the CC board.
CC	CHECKSUM in PROM 4	Bad PROM on the CC board.
CC	UREQ - TCB ERROR UREQ - INCORRECT CMD IN TCB	These errors indicate a CC board problem in the Transmit Character Buffer (TCB) in the DDT.
	UREQ - UREQ INT WITH UREQ FLAG OFF	The status of the UREQ flag must be cleared, before the UREQ command is executed, for the DDT to recognize the next request.
CC	DDTR/DDTW-UNEXPECTED VALUE IN TCB	Data turnaround test failed.
	DDT TIMED OUT WHILE SCANNING PROCESSOR	Scan counter is not functioning.
CC, SQ	CLOCK CONTROL	CPU Clock Check. The control Store Program Counter (CSPC) did not increment when a clock was issued.
CC	DDT RAM	RAM parity error in DDT RAM.

Failed Board	Error Message	Description
CC, PMI, OSP	BAD COMMAND FROM OSP	DDT detected an erroneous OSP command.
CC, PMI, OSP	DDT OUTPUT BUFFER OVERFLOW	Processor sent a message that was greater than 1K in length.
CC	UNEXPECTED INTER-RUPT CHANNEL 0	CTC channel 0 interrupted when it should not be.
CC	NMI - RAM PARITY NOT ON	When the DDT processed an NMI, the RAMPERR flag was not on. (NMI is used only for RAM parity errors.)
	ERROR FREEZE ON COLD LOAD	Error freeze occurred during HCS Load. Check Processor Status Screen for Parity Errors. Run General Diagnostics.
MM 0-3	NO MEMORY	DDT did not find any memory.
CC	SCAN PATHS ERROR	Path from DDT to scan strings is unavailable.
CC	SCAN COUNTER ERROR	Counter is not incrementing.
CC	UART TIMEOUT	UART failure
CC	SCAN STRING CC A	Specified string has failed the scan string test.
CC	SCAN STRING CC B	" "
IP	SCAN STRING IP A	" "
IP	SCAN STRING IP B	" "
MC	SCAN STRING MC A	" "
MC	SCAN STRING MC B	" "
SQ	SCAN STRING SQ A	" "
SQ	SCAN STRING SQ B	" "
SQ	SCAN STRING SQ C	" "
MM 0	SCAN STRING MM 0	" "
MM 1	SCAN STRING MM 1	" "
MM 2	SCAN STRING MM 2	" "
MM 3	SCAN STRING MM 3	" "
	SCAN STRING MM 4	Check backplane modification.
	SCAN STRING MM 5	" "
	SCAN STRING MM 6	" "
	SCAN STRING MM 7	" "

Failed Board	Error Message	Description
MC	SCAN STRING MC I	Specified string has failed the scan string test.
MC	SCAN STRING MC U	" "
SQ	NOVRAM CHECKSUM for SQ	Specified NOVRAM has a bad checksum.
IP	NOVRAM CHECKSUM for IP	" "
CC	NOVRAM CHECKSUM for CC	" "
MC	NOVRAM CHECKSUM for MC	" "
MM 0	NOVRAM CHECKSUM/TYPE for MM 0	Specified NOVRAM has a bad checksum, or the board type is incorrect. Verify configuration using the F3 Processor Configuration Screen located in General Test.
MM 1	NOVRAM CHECKSUM/TYPE for MM 1	
MM 2	NOVRAM CHECKSUM/TYPE for MM 2	
MM 3	NOVRAM CHECKSUM/TYPE for MM 3	" "
	NOVRAM CHECKSUM/TYPE for MM 4	Check backplane modification.
	NOVRAM CHECKSUM/TYPE for MM 5	" "
	NOVRAM CHECKSUM/TYPE for MM 6	" "
	NOVRAM CHECKSUM/TYPE for MM 7	" "
MM 0	STRING SELECTION - MM 0	This board failed the string selection test. More than one board may be responding to this scan string.
MM 1	STRING SELECTION - MM 1	" "
MM 2	STRING SELECTION - MM 2	" "
MM 3	STRING SELECTION - MM 3	" "
	STRING SELECTION - MM 4	Check backplane modification.
	STRING SELECTION - MM 5	" "
	STRING SELECTION - MM 6	" "
	STRING SELECTION - MM 7	" "
MM 0	SERIAL No. for MM 0	Serial Number for this board is incorrect. This may be a bad NOVRAM; more than one board may be responding to scan string.
MM 1	SERIAL No. for MM 1	" "
MM 2	SERIAL No. for MM 2	" "
MM 3	SERIAL No. for MM 3	" "

Failed Board	Error Message	Description
	SERIAL No. for MM 4	Check backplane modification.
	SERIAL No. for MM 5	" "
	SERIAL No. for MM 6	" "
	SERIAL No. for MM 7	" "
MM 0	NOVRAM COUNT for MM 0	The NOVRAM on the specified board has exceeded the number of times it should be written.
MM 1	NOVRAM COUNT for MM 1	" "
MM 2	NOVRAM COUNT for MM 2	" "
MM 3	NOVRAM COUNT for MM 3	" "
	NOVRAM COUNT for MM 4	Check backplane modification.
	NOVRAM COUNT for MM 5	" "
	NOVRAM COUNT for MM 6	" "
	NOVRAM COUNT for MM 7	" "
SQ	NOVRAM WRITE for SQ	DDT tried to write the specified NOVRAM, but the read-back check failed.
IP	NOVRAM WRITE for IP	" "
CC	NOVRAM WRITE for CC	" "
MC	NOVRAM WRITE for MC	" "
MM 0	NOVRAM WRITE for MM 0	" "
MM 1	NOVRAM WRITE for MM 1	" "
MM 2	NOVRAM WRITE for MM 2	" "
MM 3	NOVRAM WRITE for MM 3	" "
	NOVRAM WRITE for MM 4	Check backplane modification.
	NOVRAM WRITE for MM 5	" "
	NOVRAM WRITE for MM 6	" "
	NOVRAM WRITE for MM 7	" "

5.1.2.3 Current DDT State Field

The Current DDT State field displays the state of the DDT flags to verify the proper operation of the UART, and the state of the reset enable switch on each processor in the system.

RESET STATE: PMI Reset Enable switch is either in enable or disable position.

TCB STATE: DDT Transmitter Character Buffer that holds the transmit data to be sent from the DDT to the OSP is either empty and ready to accept another character, or full.

RCB STATE: DDT Receiver Character Buffer that holds the receive data to be sent from the DDT to the IP is either full with a character available to sent to the IP, or empty.

OVERRUN STATE: Either clear, or there is an RCB overrun. If the IP fails to accept an RCB character before the DDT receives the next noncommand character, the character is overwritten and the OVERRUN flag is set. An IP character acknowledge causes the DDT to clear the OVERRUN, allowing the next character to be loaded into the RCB.

5.1.3 Diagnostics

The following documents are required to run NonStop TXP Diagnostics:

a. CPU1432, NonStop TXP Diagnostic Operating Procedures, Part Number 82804, Volume 1, Chapter 1.

b. MEM2432, NonStop TXP Diagnostic Operating Procedures, Part Number 82804, Volume 1, Chapter 2.

5.1.3.1 Processor General Test Diagnostic (CPU1432)

The Processor General Test diagnostic is designed to verify the proper functioning of the processor portion of the subsystem. When the processor or processors are generating errors, Processor General Test can be run to determine the error type and to isolate the failure to the board level. This test assumes that the processor DDT and the OSP are both functional.

The Processor General Test diagnostic resides on one of the two floppy diskettes associated with the OSP and is run through the OSP. When loaded, the Diagnostic Control Screen on the OSP offers two capabilities for running the battery of tests included in the NonStop TXP General Processor Test (CPU1432), the Automatic Sequence and the Manual Sequence.

The Automatic Sequence provides five test sequences, or command groups, the first of which runs in all instances automatically, the other four of which may be selected in various combinations; all are operator selectable from the Diagnostic Control Screen. In this sequence, testing always begins with Test A, the Basic Processor Verification Test. Succeeding tests may be selected; however, Test E, the Memory Control Unit Test is always preceded by Test B, the Cache/ Address Translator Test.

The Automatic Sequence provides safeguards to prevent the operator from testing the processor in an inappropriate order. These safeguards do not exist in the Manual Sequence; it is the responsibility of the operator to insure proper sequencing.

In the Manual Sequence, the operator may select any one of the five tests from the menu in any order. Although Test A is the default test until the operator enters another option and presses function key F12, it need not be run; nor does Test B need to precede Test E.

5.1.3.2 Memory Test Diagnostic (MEM2432)

The Memory Test Diagnostic contains a set of tests designed to verify the proper functioning of the memory subsystem. This subsystem contains up to four 2-MB memory boards. When the memory board or boards are generating errors, the Memory Diagnostic can be run to determine the error type and to isolate the failure to the chip level. Since the chips are soldered and not socketed, the CE replaces the entire board when uncorrectable memory errors are occurring. After the faulty board or boards are replaced, the diagnostic can be run again as a final test to ensure that the memory errors are eliminated. The Memory Test Diagnostic also resides on one of the two floppy diskettes associated with the OSP and is run through the OSP.

The Memory Diagnostic provides four discrete test sequences, selectable from the OSP Diagnostic Control Screen. These include both a quick and comprehensive memory test, a routine that returns the memory configuration, and a power fail test.

The Memory Diagnostic requires a functioning OSP subsystem. Given that, it proceeds on two assumptions about the operational state of the processor under test:

a. That the DDT has, at power-on, successfully performed basic shift string verification of the memory boards.

b. That the Memory Control (MC) board has been verified along with processor internal functions by the Processor General Test diagnostic.

5.2 PREPARATIONS FOR REMOVAL AND REPLACEMENT

Before a defective FRU can be replaced, the following procedures for taking the processor module and the IPB off line are required.

5.2.1 Processor Module

The following paragraphs give detailed instructions for taking a processor module off line from either the Command Interpreter or OSP, and bringing it back on line after repairs have been made.

5.2.1.1 Taking a Processor Module Off Line

Inform the system manager of your need to have a processor taken off line. The system manager will do the following prior to taking the processor off-line:

a. Ensure that user processes currently running in the processor remain operational when the processor module is taken off line.

   1. Execute the COMINT command STATUS <cpu #> to list all processes running in that CPU, whether named or not.

   2. Execute the COMINT command PPD to determine which processes are not running NonStop.

   3. If there are any user processes operating without backup in the processor to be taken off line, the system manager can authorize their termination or arrange for them to be restarted in another processor.

   4. Execute the PUP command REFRESH to ensure that the File Labels represent the actual status of files on disc.

NOTE

When a processor is taken off line, all NonStop processes currently active in that processor automatically switch to the assigned backup processor.

b. Transfer to another processor the path preference of all controllers whose preferred path is currently assigned to the processor to be taken off line. The procedure is as follows:

   1. Execute the PUP command LISTDEV to determine which controllers currently have preferred paths assigned in the processor to be taken off line.

   2. For all affected controllers, execute the PUP command PRIMARY to reassign the preferred path to the backup processor.

   3. Exercise all affected devices to verify that the newly assigned path is operational.

   4. Re-execute the PUP command LISTDEV to verify that the switch takes place.

   5. Remove the processor from the poll list on the OSP by depressing the shifted F5, select the processor to be removed from the poll list on the OSP screen, then depress the unshifted F1 to initiate the action.

   6. Go to the operator panel of the processor to be taken off line. Insert the processor key in the RESET/LOAD key switch and turn the key to the RESET position. The control panel light then goes out and a message is logged at the system console acknowledging that the processor is off line.

A processor selected by the OSP (using shifted F6) may also be halted from the OSP with the unshifted F15 function key. This allows the operator to place the selected processor into the local halt state. LHLT (Local Halt) then appears on the screen for that processor. (To exit this mode, press the shifted function key F1 to return control of the terminal to the Command Interpreter.)

5.2.1.2 Powering-up a Processor Module

Power up a processor as follows:

a. Apply DC power to the processor module by placing the 115/230 VAC power and DC power switches on the associated DC Power Module in the ON (up) position. See Figure 5-2 for the location of the switches.

b. Reload the processor.

5.2.1.3 Reloading a Processor Module

This procedure is used to bring a processor module back into operation in an otherwise operational system. The procedure, using a Command Interpreter, is as follows:

a. On the control panel for the processor module to be reloaded, set switch register <0> to the UP position and all other switches down.

b. On the same control panel, turn the key in the RESET/LOAD switch to the RESET position, wait for all control panel lights to light, and then turn the key to the LOAD position. (The control panel lights will go to %177777 after RESET and to 0 after LOAD.

c. Using a Command Interpreter, enter the following command:

```
:RELOAD <cpu> [, $<volume name> , {0:1}]
```

Where: <volume name> is the name of a volume containing <cpu> operating system image.

If the reload is successful the switch register display LEDs show: %177777

d. Place the processor back on the poll list with the OSP by depressing the shifted F5, select the processor previously removed from the poll list, and depress the unshifted F1 to initiate the action.

5.2.1.4 Cold-loading the Processor

Cold-loading is used to bring the system into operation after one of the following:

a. The entire system has been shut down for maintenance (with the operating system images and files on disc still intact)

b. A new operating system or operating system update has been installed.

If the system is to be cold-loaded from the disc using OSP, follow the instructions provided in Section 4 of the Operations and Service Processor User Guide.

If the system is to be cold-loaded from an I/O device follow the instructions provided in the NonStop II System Operations Manual.

5.2.2 Interprocessor Bus

After cold-loading a processor, it is recommended that both the X and Y Buses be checked for proper operation.

The following paragraphs give instructions for taking an IPB off line and bringing it back on line after repairs and cold-load have been completed.

5.2.2.1 Taking an Interprocessor Bus Off Line

To take a Interprocessor Bus off line, do the following:

a. Have the system manager select a terminal with an executing Command Interpreter and enter the following command to take the desired bus off line:

```
{X|Y} BUSDOWN <from processor>,<to processor>
```

examples:

```
: X BUSDOWN 1,2
```

(down the X-Bus from processor 1 to processor 2)

```
: Y BUSDOWN -1,0
```

(down the Y-Bus from all processors to processor 0)

```
: X BUSDOWN 0,-1
```

(down the X-Bus from processor 0 to all other processors)

```
: Y BUSDOWN -1,-1
```

(down the Y-Bus from all processors to all processors)

b. The following console message is printed for the bus taken off line:

```
20 {...} X Bus to processor n DOWN (BEL)
21 {...} Y Bus to processor n DOWN (BEL)
```

5.2.2.2 Placing An Interprocessor Bus On Line

Place the appropriate bus on line as follows:

a. Using a Command Interpreter, enter the following command.

{X|Y}BUSUP <from cpu number>, <to cpu number>

b. The following console message is printed for the bus placed on line:

```
22 {...} X BUS TO PROCESSOR n UP (BEL)
23 {...} Y BUS TO PROCESSOR n UP (BEL)
```

5.3 UNPACKING REPLACEMENT BOARDS

After receiving a replacement board, perform inspection as follows:

a. Open container and remove the board from the antistatic plastic bag. Save packing material for reshipping the defective board.

b. Check for cleanliness and ensure that there is no damage to the board, particularly at the edge contacts.

5.4 REMOVAL AND REPLACEMENT PROCEDURES

Before removing any processor boards, the processor must be logically removed from the system using the procedure described in paragraph 5.2.1.1.

The following procedures include steps for removing a suspected malfunctioning board after a diagnostic routine (see paragraph 5.1.3 for diagnostics) has isolated the problem to a specific board.

5.4.1 IP, MC, CC, SQ, or MM Board

The following paragraphs explain removal and replacement procedures for the IP, MC, CC, SQ, and MM boards.

5.4.1.1 Removal

To remove any one of the boards, do the following:

a. Have the system manager take the appropriate processor module off line (paragraph 5.2.1.1).

b. Remove DC power from the processor module taken off line by placing the 115/230 VAC Power and the DC Power switches on the associated 7301 DC Power Module in the OFF (down) position. See Figure 5-2 for the location of the power supply switches.

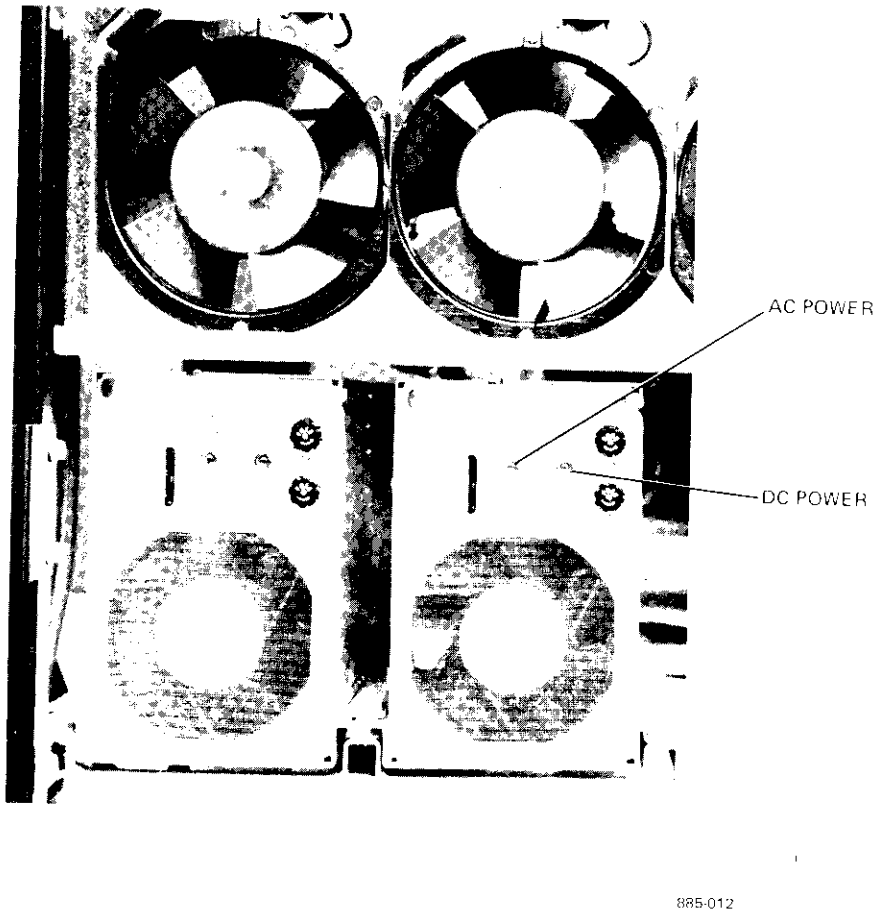


Figure 5-2 DC Power Module

c. Remove the cables from the appropriate front-edge connectors. If necessary label cables. See Figure 5-4 at the end of this Section for the board removal procedures.

d. Loosen the PCB hold-down screw in the rear of the system cabinet and carefully remove the board from the front of the cabinet.

e. See paragraph 5.4.1.2 for replacement procedure.

5.4.1.2 Installing Replacement IP, MC, CC, SQ, or MM Boards

Before replacing the defective board, inspect the replacement board for possible damage. Use the reverse procedure of board removal when installing a new board. After installing the board in the correct slot, completing the necessary cable interconnections, and restoring power, notify the system manager to place the processor on line. See Figure 5-4 at the end of this Section for the board replacement procedures.

CAUTION

Large boards should NOT be inserted in their slots using the PCB hold-down screw. Over tightening of this screw can break traces or cause seating problems. Use the hold down screw to start the board into the connectors, then push the board in from the front until it is seated into the connector. The hold down screw should only be "finger tight."

5.4.2 I/O Terminator Board

The following paragraphs explain the removal and replacement procedure for an I/O Terminator board.

5.4.2.1 Removing an I/O Terminator Board

To remove an I/O Terminator board, do the following:

a. Have the system manager take the appropriate processor module off line. See paragraph 5.2.1.1.

b. Remove DC power from the processor by placing the 115/230 VAC Power and DC Power switches on the associated 7301 DC Power Module in the OFF (down) position. See Figure 5-2.

c. Remove the I/O bus cable from J1 and the DC power cable from J2 on the I/O Terminator board.

d. Cut the cable tie that secures the board to the I/O bus cable and remove the board.

e. See paragraph 5.4.2.2 for replacement procedure.

5.4.2.2 Installing a Replacement I/O Terminator Board

To install an I/O terminator board, do the following:

a. Install the I/O bus cable to connector J2 and the DC power cable to connector J1.

b. Secure the I/O terminator to the I/O bus cable with a cable tie.

c. Apply DC power to the appropriate processor module in accordance with paragraph 5.2.1.2.

d. Verify that the power indicator LED is lit.

e. Reload the processor in accordance with paragraph 5.2.1.3.

5.4.3 Operator Control Panel Assembly

The following paragraphs describe how to remove and install a replacement operator control panel assembly.

5.4.3.1 Removing an Operator Control Panel Assembly

To remove an operator control panel assembly, do the following:

a. Have the system manager take the appropriate processor module off line (see paragraph 5.2.1.1.)

b. Remove DC power from the processor taken off line by placing the 115/230 VAC Power and DC Power switches on the associated DC Power Module in the OFF (down) position. See Figure 5-2.

c. Remove the flat ribbon cables from the control panel.

d. Remove the three slotted screws that secure the assembly to the front door of the system cabinet.

e. Remove the control panel assembly.

f. See paragraph 5.4.3.2 for replacement procedure.

5.4.3.2 Installing a Replacement Operator Control Panel

See paragraph 5.4.3.1 and install the control panel in the reverse order of steps c) and d).

a. Apply DC power to the appropriate processor module in accordance with paragraph 5.2.1.2.

b. Reload the processor in accordance with paragraph 5.2.1.3.

5.4.4 IPB Controller Boards

The following paragraphs describe how to remove and install a replacement IPB controller board.

5.4.4.1 Removing an IPB Controller Board

To remove an IPB Controller board, do the following:

a. Have the system manager take the bus to which the IPB Controller is attached off line (paragraph 5.2.2.1). The <from processor> and <to processor> parameters must be specified as -1 to take the entire bus off line.

b. Turn off DC power by placing the power switch on the power regulator card for this controller in the OFF (down) position.

c. Remove the bus cable from connector J1. Remove the DC power cable from connector J2. Remove and label the CPU select cables from connectors J100 through J115.

d. Release the plunger latch in the upper right-hand corner of the board.

e. Remove the two slotted screws that secure the board to the stand-offs. Carefully remove the board.

f. See paragraph 5.2.1.3 for replacement procedure.

5.4.4.2 Installing a Replacement IPB Controller Board

To replace an IPB Controller board, do the following:

a. Install the replacement board by securing it to the stand-offs with two slotted screws. Engage the plunger latch.

b. Install the bus cable to connector J1 and the DC power cable to connector J2. Install the CPU select cables to connectors J100 through J115.

c. Apply DC power by placing the power switch on the power regulator card for this controller in the ON (up) position.

d. Place the bus that the IPB Controller is attached on line. See paragraph 5.2.2.2. The <from processor> and the <to processor> parameters must be specified as -1 (bring up the entire bus).

5.4.5 IPB Terminator Boards

The following paragraphs describe how to remove and install a replacement operator IPB terminator board.

5.4.5.1 Removing an IPB Terminator Board

To remove an IPB Terminator board, do the following:

a. Have the system manager take the bus to which the IPB Terminator is attached off line (see paragraph 5.2.2.1). The <from processor> and <to processor> parameters must be specified as -1.

b. Remove the bus cable from J1 on the IPB Terminator Board and remove the board.

c. See paragraph 5.4.5.2 for replacement procedure.

5.4.5.2 Installing a Replacement IPB Terminator Board

To replace an IPB Terminator board, do the following:

a. Take the appropriate bus off line (X or Y Bus) in accordance with paragraph 5.2.2.1.

b. Install the replacement IPB Terminator board to the stand-offs and secure it with the two slotted screws.

c. Install the bus cable to connector J2 on the IPB Terminator board.

d. Place the appropriate bus on line (X or Y Bus) (paragraph 5.2.4.2). The <from processor> and <to processor> parameters must be specified as -1.

5.5 PACKAGING DEFECTIVE BOARDS FOR RESHIPPING

After the new board has been installed, pack the defective board for shipment, using the packing material from the new board.

a. Each board should be protected in a separate plastic antistatic bag, and reshipped in the same packing in which the replacement board was received, between two layers of foam packing.

> CAUTION
>
> Do not stack two or more boards in the same box, since this can cause irreparable damage to the boards.

b. To prevent damage from handling, there should be at least a two-inch space between the board edges and the sides of the container.

c. More than one board may be shipped in a large container provided adequate packing is used to keep them separated.

d. The box must be closed securely with tape. Boxes may be taped together for cost effective shipping. For information concerning shipping companies and their particular requirements, refer to the Shipping Guide Bulletin available from the TANDEM Shipping Dept., Cupertino.

e. To avoid confusion, remove or cover all addressing information used in previous shipping. This includes airport codes or destination stamps.

5.6 DOCUMENTATION USED IN RESHIPPING

When returning a defective NonStop TXP part for repair, fill out an Incident Report (IR) Form (99751) and a Part Return Tag (99056). Attach the Part Return Tag to the defective part. Send the IR along with the defective part to Customer Engineering Headquarters, Department 744, located at 2450 Walsh Avenue, Santa Clara, CA. 95050.

When returning a CPU board, please report on the IR the type of error, the error symptoms, and the conditions under which the error occurred. The IR should contain information as displayed by the Processor Status Screen, along with the results of the diagnostic tests. Specifically report the following conditions on the Incident Report:

a. Rank 1 and Rank 2 Address Errors, or Rank 4 Addresses.

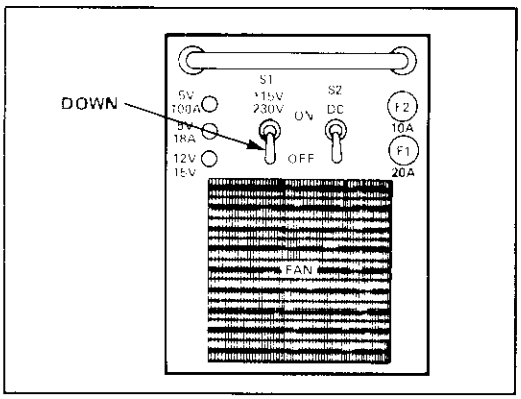
b. DDT Indicator Codes.

c. DDT Detected Errors.

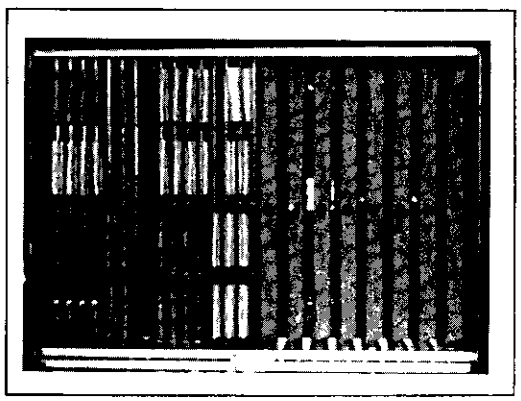
d. Parity Errors on the Procesor Status Screen.

e. Control Panel Light Indications.

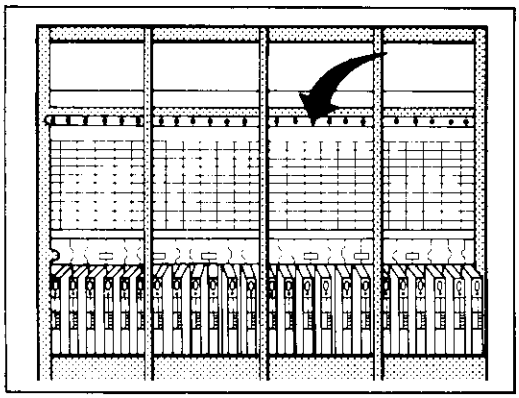
f. Results of Diagnostics tests.



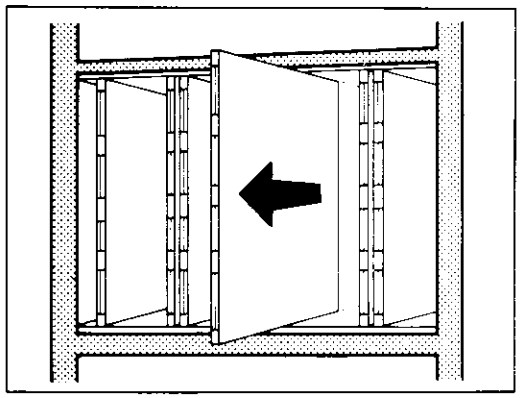
1. TURN OFF POWER TO THE APPROPRIATE PROCESSOR.



2. DISCONNECT THE FLAT RIBBON CABLES FROM THE FRONT EDGE CONNECTORS.



3. LOOSEN SCREW AT THE REAR OF THE CABINET.



4. GENTLY PULL BOARD OUT FROM THE CABINET.

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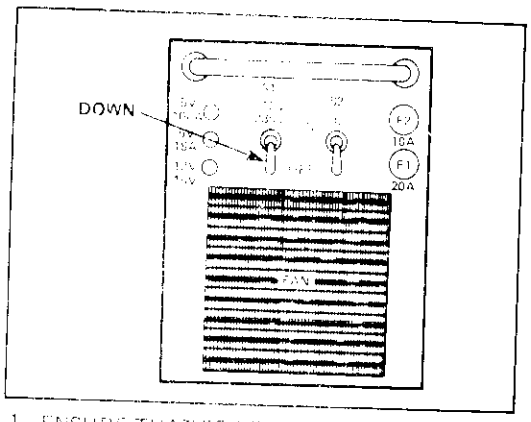
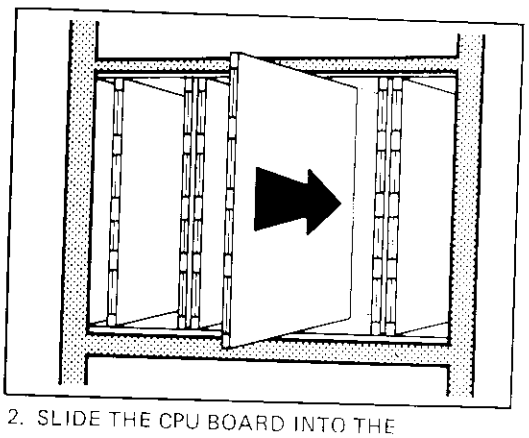
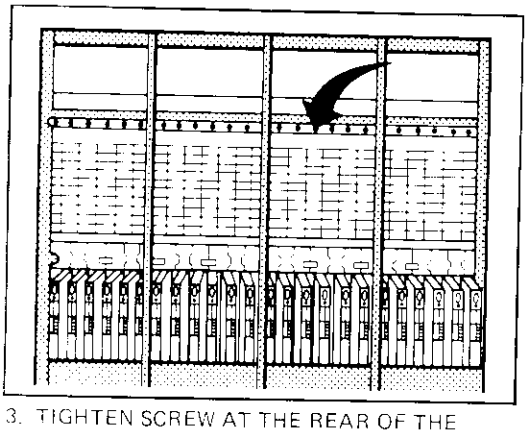
Figure 5-3 Board Removal Procedure



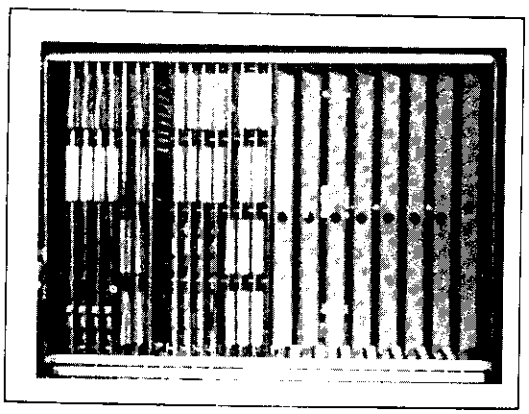
1. ENSURE THAT POWER IS OFF TO THE APPROPRIATE PROCESSOR.



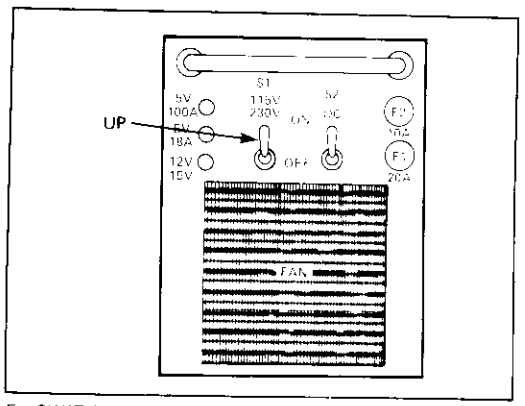
2. SLIDE THE CPU BOARD INTO THE APPROPRIATE CARD SLOT. TURN SCREW AT REAR OF CABINET UNTIL ENGAGED. PUSH BOARD IN FROM FRONT UNTIL IT IS SEATED.



3. TIGHTEN SCREW AT THE REAR OF THE CABINET UNTIL "FINGER TIGHT".



4. CONNECT THE FLAT RIBBON CABLE TO FRONT EDGE CONNECTORS.



5. SWITCH ON POWER TO THE PROCESSOR.

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Figure 5-4 Board Replacement Procedure

SECTION 6
PREVENTIVE MAINTENANCE

6.0 PREVENTIVE MAINTENANCE

During regular system preventive maintenance, check the processor boards for loose cables, verify that each board is firmly seated in the cabinet, and verify that all connectors are fastened securely.

6.1 CHECK OPRLOG

During normal preventive maintenance, check the system OPRLOG to see if there are excessive errors listed for the NonStop TXP Processor.

SECTION 7
SPECIAL TOOLS AND TEST EQUIPMENT

7.0 SPECIAL TOOLS AND TEST EQUIPMENT

Special tools or test equipment are not required for the NonStop TXP Processor.

SECTION 8
FIELD REPLACEABLE UNITS

8.0 FIELD REPLACEABLE UNITS

The following Tables and Figures list the part numbers and show the location of the field replaceable units for both the NonStop TXP processor subsystem and NonStop II systems that have been modified to accept the NonStop TXP. The part lists, divided into four sub-groups for easier referencing, are:

a. Field Replaceable CPU Boards

b. NonStop TXP CPU Interconnect Cables

c. NonStop TXP/NonStop II Field Replaceable Units

d. NonStop TXP/NonStop II Cabinet Modification Parts.

8.1 FIELD REPLACEABLE CPU BOARDS

Table 8.1 lists the field replaceable CPU boards for the NonStop TXP processor, and Figure 8-1 shows the board location.

Table 8.1 NonStop TXP Field Replaceable CPU Boards

REFERENCE NUMBER	PART NUMBER	DESCRIPTION
2	59640	(SQ) SEQUENCER AND CONTROL STORE
3	59630	(CC) CHANNEL AND CONTROL
1	59620	(IP) INSTRUCTION PROCESSOR
4	59610	(MC) MEMORY CONTROL
5	59600	(MM) MEMORY ARRAY RAM (2 MB)

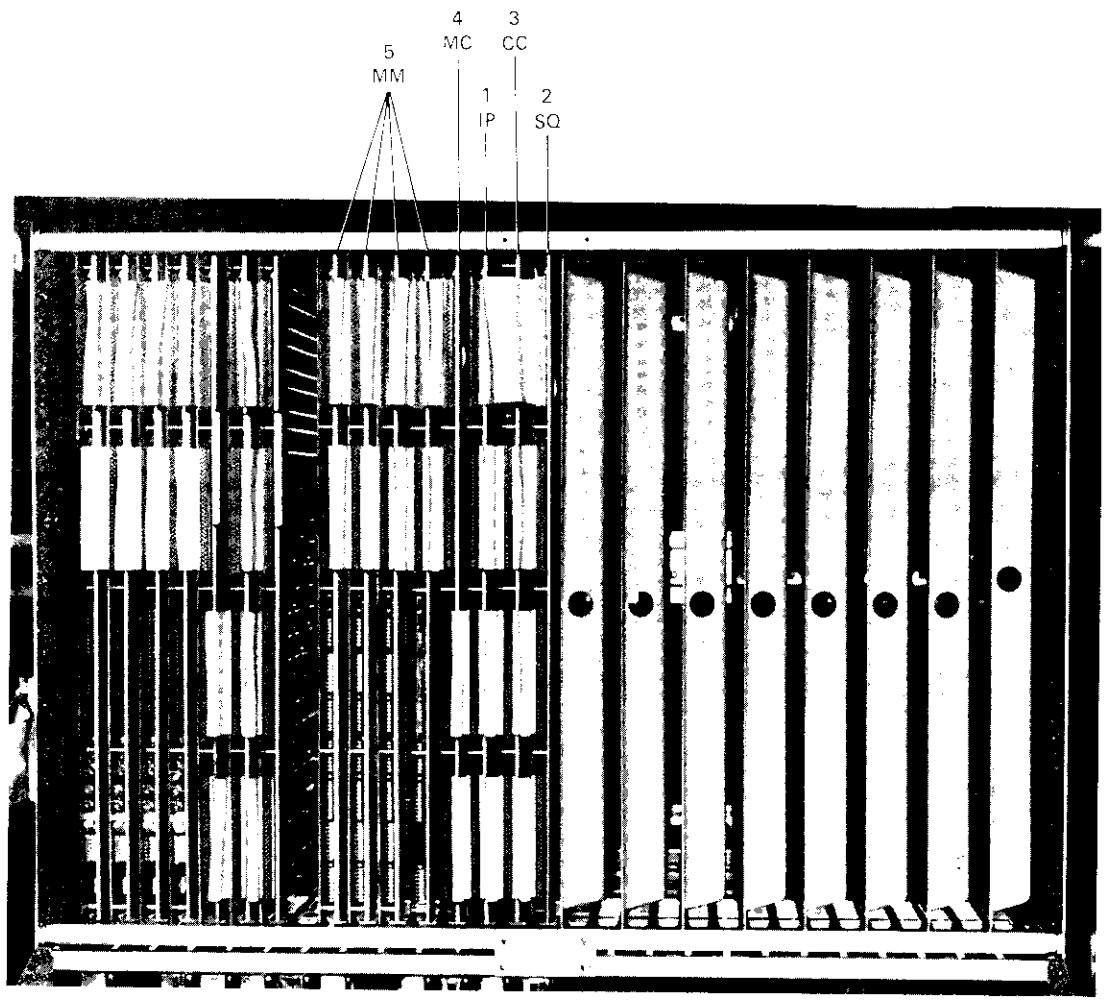

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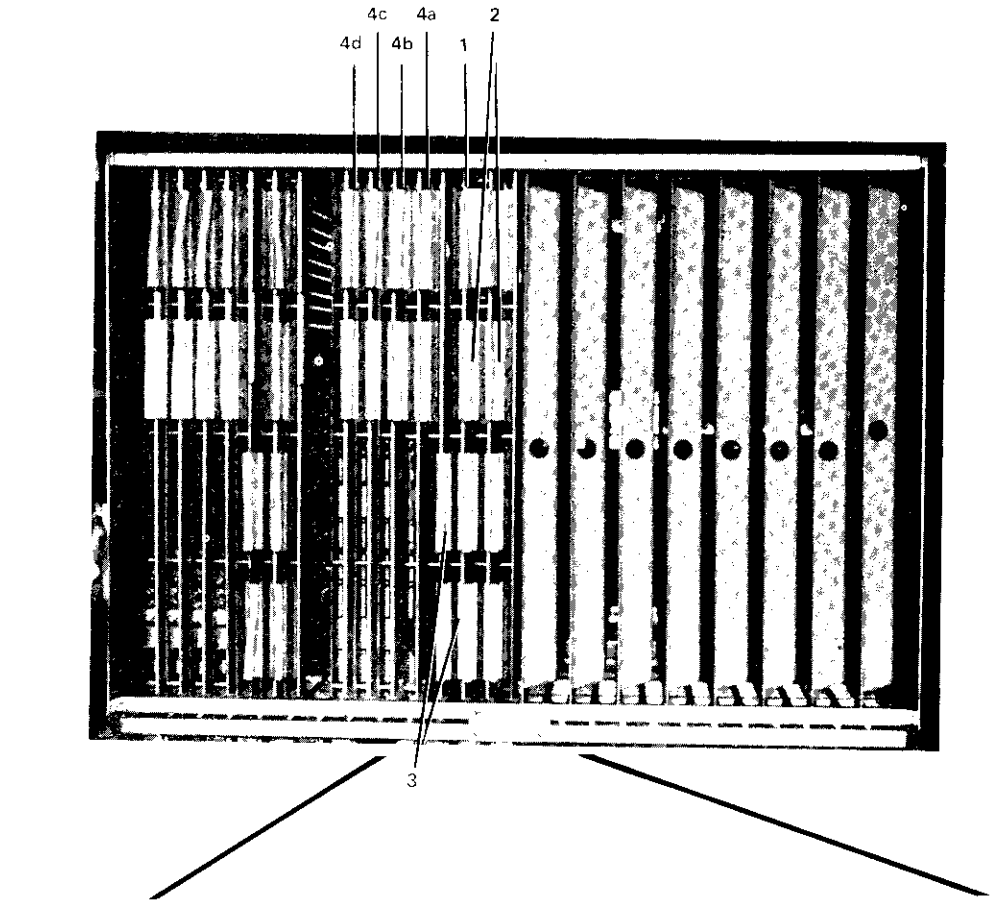
Figure 8-1 NonStop TXP CPU Board Locations

8.2 NonStop TXP CPU INTERCONNECT CABLES

Table 8.2 lists the CPU interconnect cables and Figure 8-2 shows the locations of the cables on the CPU boards.

Table 8.2 NonStop TXP CPU Interconnect Cables

ITEM NO.	DESCRIPTION	J NUMBER	PART NUMBER
1	CBA IP-SQ	J1	59996
2	CBA IP-CC-SQ	J2	55662
3	CBA MC-IP-CC-SQ	J3-J4	55663
4a	CBA MC-MM/X1: Used with one 2MB board	J1-J2	55661
4b	CBA MC-MM/X2: Used with two 2MB boards	J1-J2	55662
4c	CBA MC-MM/X3: Used with three 2MB boards	J1-J2	55663
4d	CBA MC-MM/X4: Used with four 2MB boards	J1-J2	55664



BOARD	MM	MM	MC	IP	CC	SQ
SLOT	MEM	MEM	MCB	IPU	CCD	OPT
2	3	4	5	6	7	8
10	11	12	13	14	15	16
18	19	20	21	22	23	24

Figure 8-2 Interconnect Flat Cable Locations

8.3 NonStop TXP/NonStop II FIELD REPLACEABLE UNITS

Table 8.3 lists the field replaceable units for the NonStop TXP processor subsystem, and a processor system comprising both NonStop TXP and NonStop II CPUs.

Table 8.3 NonStop TXP and NonStop II Parts

DESCRIPTION	PART NO.
Processor Power Supply ASM 7900	53270
I/O-Only P/S ASM 7301 (115 V)	52730
I/O-Only P/S ASM 7301 (230 V)	52875
I/O Regulator	54600
I/O Bus Cable:	
TAB DRAWING	56607
Left to Right, 4 Slot	56115
Left to Right, 6 Slot	56114
Left to Right, 8 Slot	56117
TAB DRAWING	56608
Right to Left, 4 Slot	56119
Right to Left, 6 Slot	56118
Right to Left, 8 Slot	56121
I/O Bus Terminator	51440
I/O Lower Backplane 12 inch Wire (For use in backplane modification to reach odd-numbered V-tabs)	56548
PMI Panel Assembly (previously 45029)	42517
PMI Patch Panel (previously 45025)	42516
PMI PWA (previously 55330)	42470

Table 8.3 NonStop TXP and NonStop II Parts (Cont'd)

DESCRIPTION	PART NO.
PMI PWB (previously 55332)	42472
PMI Processor Cable Assembly	55521
IPB Controller with 10 MHz Crystal	57830
IPB Controller with 13 MHz Crystal	57840
Plenum Diode Assembly	59790
IPB Clock Cable:	
TAB DRAWING	42443
6.5 ft (1 or 2 cabinet system)	42444
14 ft (3 to 5 cabinet system)	42445
IPB Select Cable:	
TAB DRAWING	42440
6.5 ft (1 or 2 cabinet system)	42441
14 ft (3 to 5 cabinet system)	42442
Processor Backplane	57364 Rev B

8.4 NonStop TXP/NonStop II CABINET MODIFICATION PARTS

Table 8.4 lists the parts necessary to modify the NonStop II cabinet when installing a NonStop TXP CPU.

Table 8.4 Required Cabinet Modification Parts

DESCRIPTION	PART NO.
Plenum Diode Assembly	59790
I/O-Only P/S ASM 7301 (115 V)	52730
I/O-Only P/S ASM 7301 (230 V)	52875
Service and Maintenance Processor Board (SMP board for the Operations and Service Processor)	42540
I/O Lower Backplane 12 inch Wire (for use in backplane modification to reach odd-numbered V-tabs)	56548
30 gauge wire used in grounding backplane pins	Not Stocked